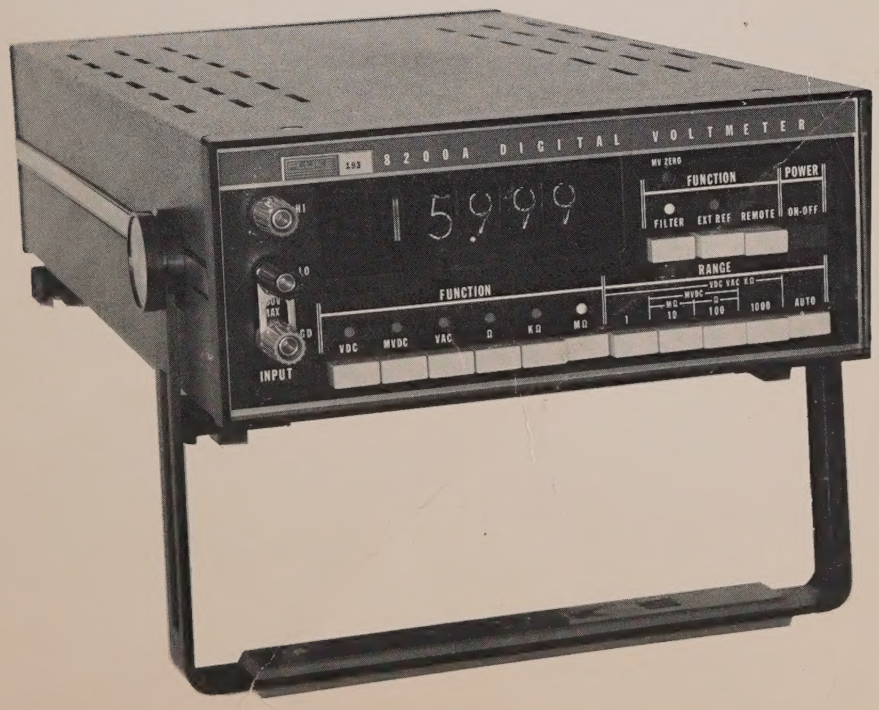
model 8200

DIGITAL VOLTMETER



FLUKE®

STUDENT HANDOUT

Introduction

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. This manual is intended as a supplement to the Audio/Visual training package of the same title. It is suggested that prior to attending this course of instruction, the course titled "Recirculating Remainder" should have been completed. Should you have any questions, comments or suggestions about this course of instruction please feel free to communicate them to the Training Department by letter or telephone.

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The rapid and efficient repair of any instrument is greatly enhanced by a thorough understanding of the theory of operation. This course is designed to fill that need for experienced technicians who are engaged in the calibration and repair of the Fluke 8200A Digital Voltmeter.

The basic 8200A is a four-digit DC voltmeter providing 1, 10, 100, and 1000 volt ranges complete with automatic polarity, automatic ranging, and 60 percent over-ranging. It comes equipped to accept a variety of options. Each of the options can be installed in the field. The options available include the:

The –01 AC Converter Option provides four AC ranges with 30 Hz to 100 kHz response. Auto-ranging from the 1 VAC range to the 1000 VAC range is provided.

The –02 Millivolt DC Option provides two ranges of millivolt measurement; a 10 mV range and a 100 mV range. It provides automatic polarity, and the instrument will autorange down into the 100 or 10 mV range, from the VDC ranges. Autorange up from 10 or 100 mV range to VDC ranges is also provided.

The –03 Resistance Option provides six resistance ranges from 100 ohms to 10M ohms, and it is overload fused at 30V RMS. Autoranging has been included in the Resistance Option.

The –04 Isolated External Reference option; it is necessary that the instrument be provided with an –05 Option, which is the Rear Input option, when an Isolated External Reference Option is installed because of the limitation of the three front panel terminals. The Isolated External Reference will provide four terminal measurements: real-time ratio determinations, DC to DC in four ranges in the basic instrument, and AC and millivolt ratios when the options are installed.

The –05 rear input option provides a five-pin connector. Offering Signal HI and LOW, Guard, and External Reference HI and LOW.

The –06 Printer Output Option provides digits, polarity, and range information. Digits information and range information is given in Binary Coded Decimal format and in parallel output. The interface logic levels are +5V and 0V, and it can be used with the Remote Control Unit; –08 Option.

The –07 Data Output Option offers digits, polarity, and range in BCD format for digits and range in 8421 parallel or 4-bit serial format. The logic levels are +5V and 0V. It provides control input for an external trigger, automatic triggering, and time-outs enabled or disabled. It can be used with the 08 Remote Control Unit option. The Isolated Data Output option cannot be installed simultaneously with the 06 Isolated Printer Output option. The instrument can only accept one of the output options.

The –08 Remote Control Unit control, or program control, will interface with DTL or TTL. The Remote Control Unit requires +5V of DC at 105 mA from either the Data Output option or the Printer Output option. If the instrument is not equipped with either of these options, a special supply accessory is available, or it must be supplied from an external power supply. The Remote Control Unit option provides a remote flag, interlock protection, and address controlled by triggers.

In addition to the options provided for the 8200A, several accessories interface with the instrument. The A90 AC-DC Current Shunts, the 80F-5 High Voltage Probe, the 80F-15 High Voltage

Probe, the 80 RF Probes, and the rack-mounting hardware for either offset center or side-by-side installation.

MAIN BODY OF TEXT

BLOCK DIAGRAM

As can be seen in the block diagram (Figure 1), the instrument consists of several basic blocks; the Power Supply, Buffer, A-D Amplifier, Logic Control, Display, and the Inter-Connect assembly. Within the Power Supply four separate voltages are sourced: A +200V DC supply for the display tubes, a +15V DC, and a −15V DC operating supplies, and a +5V DC logic supply.

BUFFER (Figure 2)

The Buffer is an operational amplifier with a gain of one inverted. If the Buffer sees a +1V at its input terminals, it will produce a −1V at its output terminals. The primary purpose of the Buffer is isolation and impedance matching. The Buffer assembly also contains the Range Divider for DC giving division ratios of 1/1, 10/1, 100/1, and 1000/1. It contains a switchable four-pole active filter which provides losses in excess of 60 DB at 50 Hz cycles, greater than 65 DB at 60 cycles, and 100 DB or more at 200 cycles and above. The Buffer also contains its own Logic circuitry for range and function switches.

A-D ANALOG (Figure 3)

The A-D Analog assembly is made up of several circuits: the Polarity Detector and Switching circuit which provides the instrument with its automatic polarity detection and indication. It contains the Sample and Hold circuitry that is used when the instrument is initially digitizing a measurement. The +7V DC Reference Supply is also contained within the A-D Analog module, as is the Current Oscillator Modulator, the Ladders, and the Display Storage network.

LOGIC CONTROL (Figure 4)

The Logic Control contains the Constant Current Oscillator and the Counter. In addition, it also contains the Master Clock, which generates the basic timing for the instrument. The Master Clock feeds the Shift Register which generates the five timing periods; ZERO and the four digitizing periods. In addition, a Sample Oscillator is provided that feeds both the Shift Register and the Analog Control circuitry. The Sample Oscillator provides the Measure and Storage pulses. In addition, the Analog Control assembly provides gating pulses that are required for the special switching requirements in Recirculating Remainder. The Sample Oscillator also feeds the Shift Register to synchronize the start of Measurement time with the Master Clock and the Shift Register.

DISPLAY (Figure 5)

The Display assembly contains four circuit functions; Anode Strobing, Polarity Memory, Decoder Driver, and the Display. Anode Strobing, using the timing pulses from Logic Control, turns the display tubes ON in the proper sequence. The Polarity Memory circuit is a bi-stable multivibrator that receives information from the Polarity Sensing circuits in the Buffer, and holds that information in "memory" until it is displayed. The Decoder Driver is a sixteen state, monolithic device used to translate the Binary Coded Decimal information from the Counter, into decimal information to be used in order to ionize the proper digit in each display tube. The Display circuitry consists of the various interconnections required for supporting the illuminated display tubes and lights.

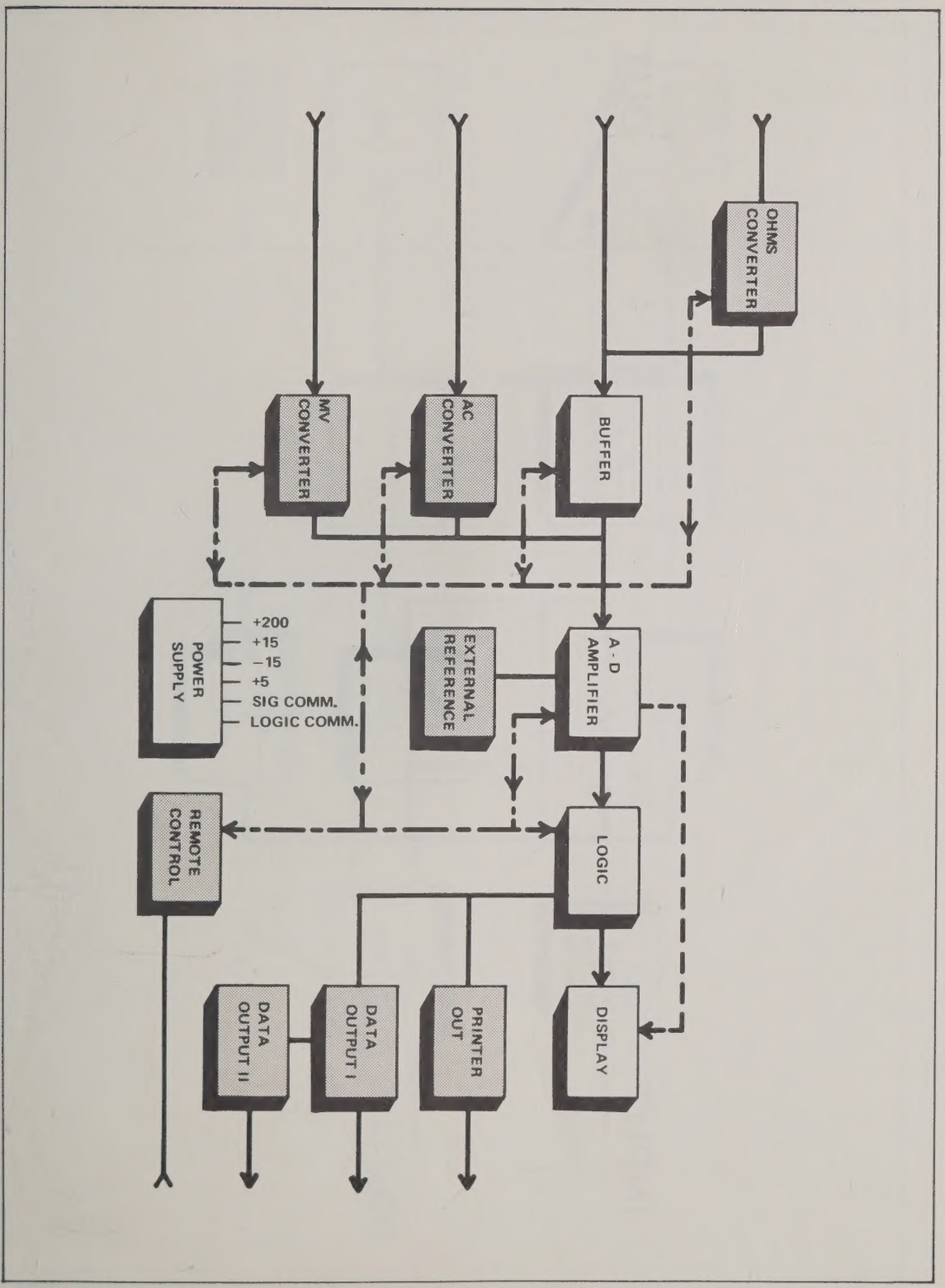


Figure 1. BASIC 8200A

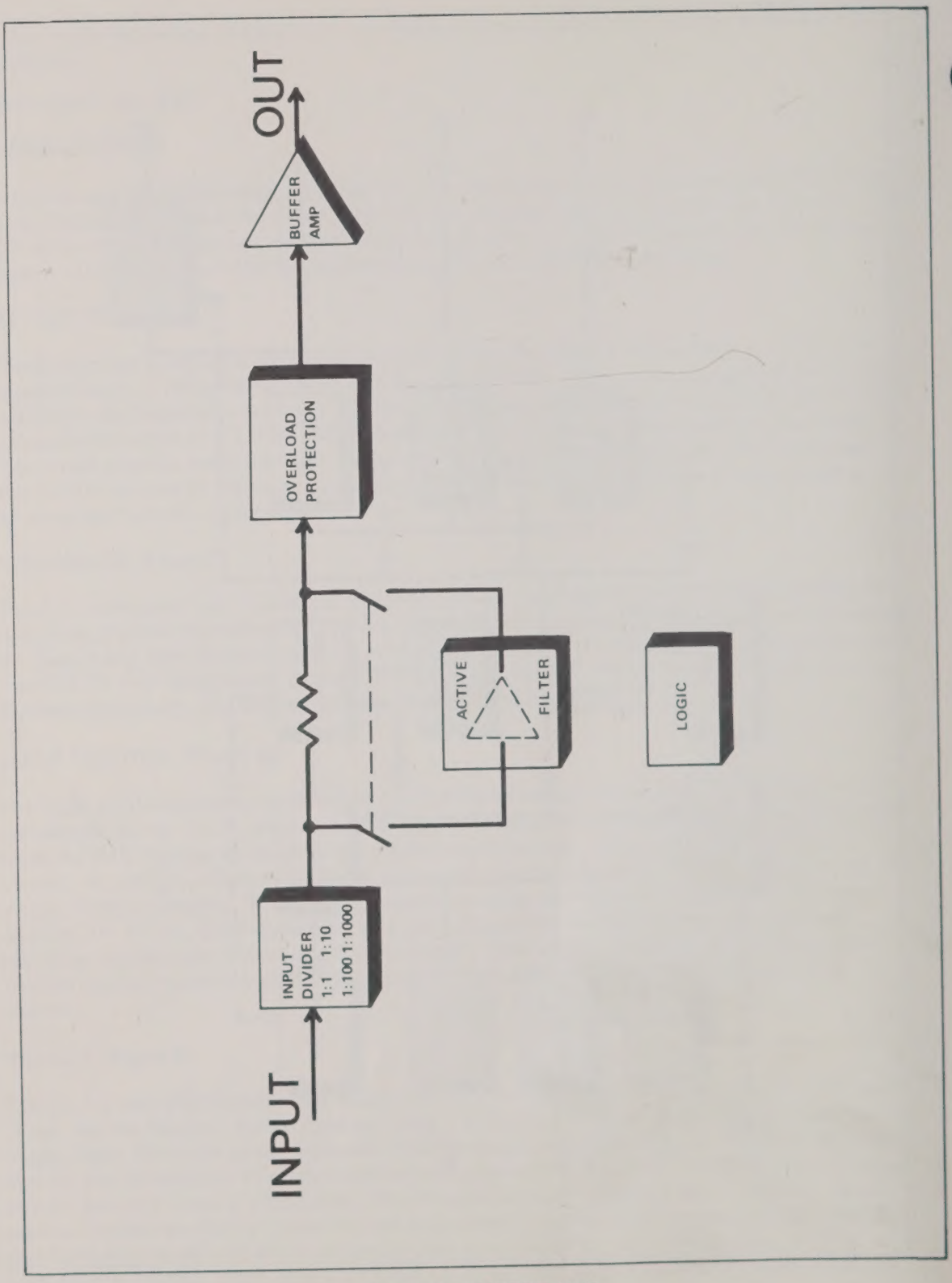


Figure 2. BUFFER (A4)

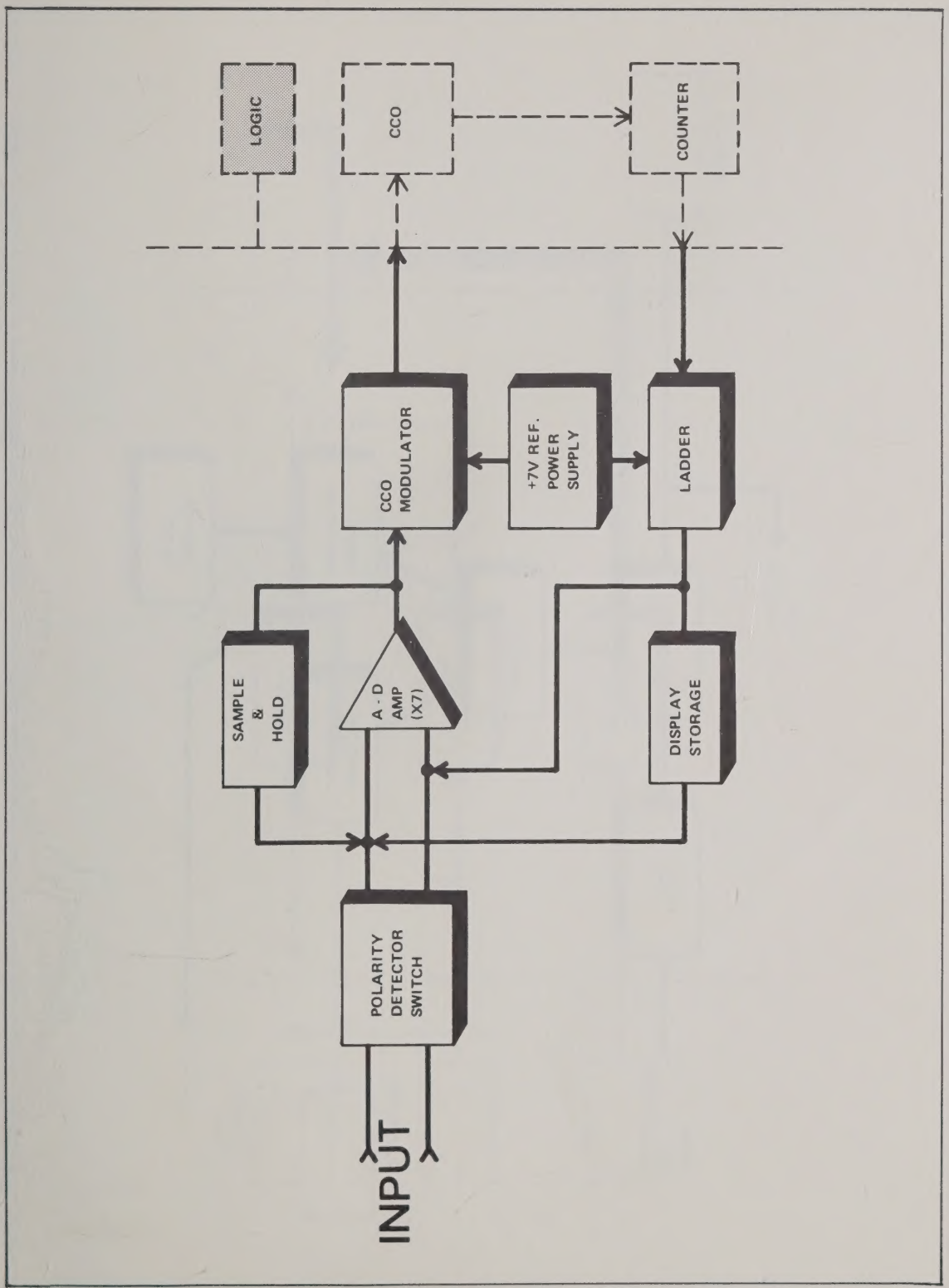


Figure 3. A TO D ANALOG (A7)

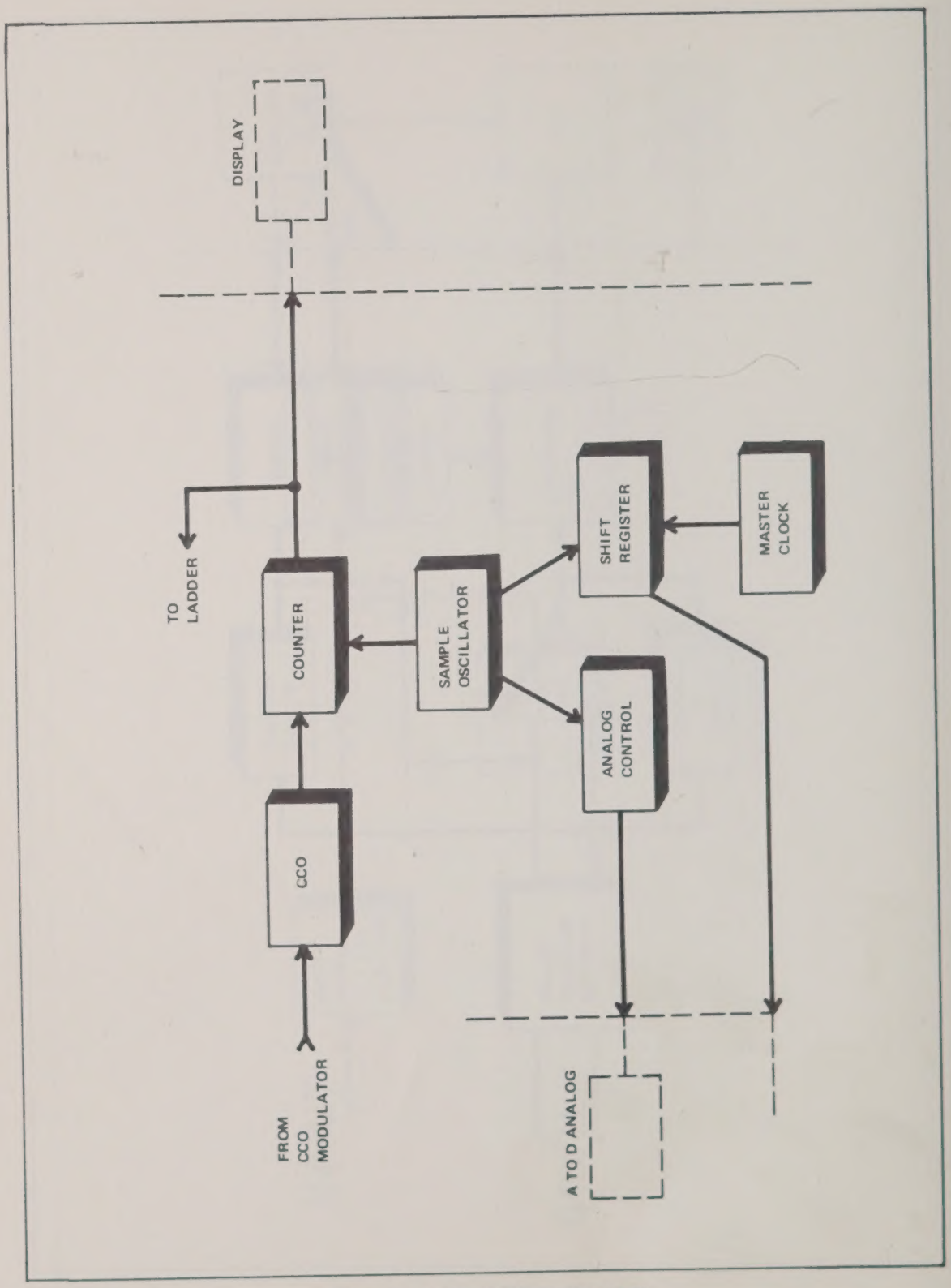


Figure 4. LOGIC CONTROL (A6)

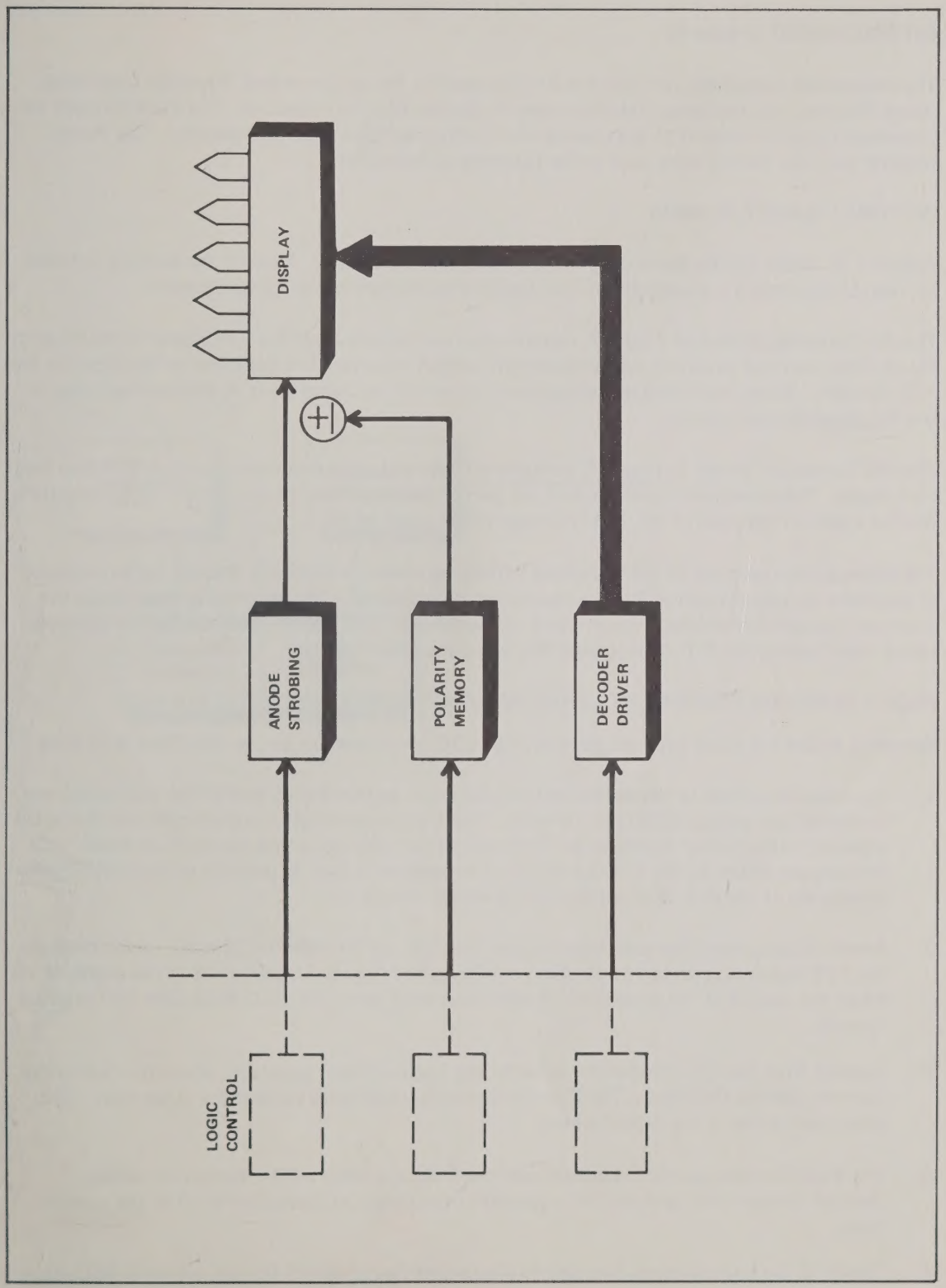


Figure 5. DISPLAY (A12)

INTERCONNECT (Figure 6)

The Interconnect assembly contains the circuits used for Range Command, Function Command, Range Register, and the Lamp Assembly used to display function selection. The Function and Range Command circuitry consists of the manual push-button switches used for selection. The Range Register contains the circuitry used in the autoranging functions.

OPTIONS (Figures 7, 8, and 9)

Figures 7, 8, and 9 are the block diagrams of the Option assemblies. Each of the options contains its own Logic circuitry, in addition to the circuitry to support its functional purpose.

The AC Converter, shown in Figure 7, contains two operational amplifiers; one used in the input to the rectifier, and one which is used to match the output impedance of the Filter to the input to the A/D circuitry. Range switching is accomplished by switching the resistors in the feedback loop of the AC operational amplifier.

The MV Converter, shown in Figure 8, contains a Filter and an operational amplifier with two feedback loops. These feedback loops control the gain of the amplifier. In the 10 mV range the amplifier has a gain of 100, and in the 100 mV range it has a gain of 10.

The Ohms option uses the +7 volt reference voltage, as shown in Figure 9, through series resistors to develop a voltage across the Rx or resistance to be measured. The resulting voltage across the unknown resistor is translated into an ohms measurement. This option feeds the Buffer assembly rather than feeding the A/D Analog assembly as do the other Options.

BLOCK DIAGRAM EXAMPLE VOLTAGE MEASUREMENT

Referring to the full block diagram given in Figure 10, the operation can be described as follows:

1. The input is applied to the buffer and divided down so that the output of the attenuator will be within the range of ZERO to 1.6 volts. The Filter is selected or not selected and the signal is passed to the Buffer Amplifier which has a gain of one and whose output is inverted. It is the purpose of the Buffer to keep the input impedance as high as possible while matching the impedance of the A-to-D Amplifier circuit which follows it.

2. A-to-D Analog Amplifier assembly receives the signal at the Polarity Detector which operates the FET switches applying the proper polarity to the A-to-D Amplifier which has a gain of 70. When the output of the amplifier is greater than the 7 volts, the CCO Modulator will produce current.

3. Current from the CCO Modulator is fed to the Logic Control assembly, where it is fed to the Current Control Oscillator. The Current Controlled Oscillator produces a pulse train. This pulse train is fed to the BCD Counter.

4. The BCD Counter counts the pulses from the CCO and feeds BCD information to the Decoder Driver which will furnish a ground to the proper numeral line to all of the display tubes.

5. The BCD Counter output is also fed to the Ladder Switches and Drivers and each BCD count causes the Ladder outputs to advance by 0.1 a volt. The output of the Primary Ladder is fed back to the input to the A-to-D Amplifier.

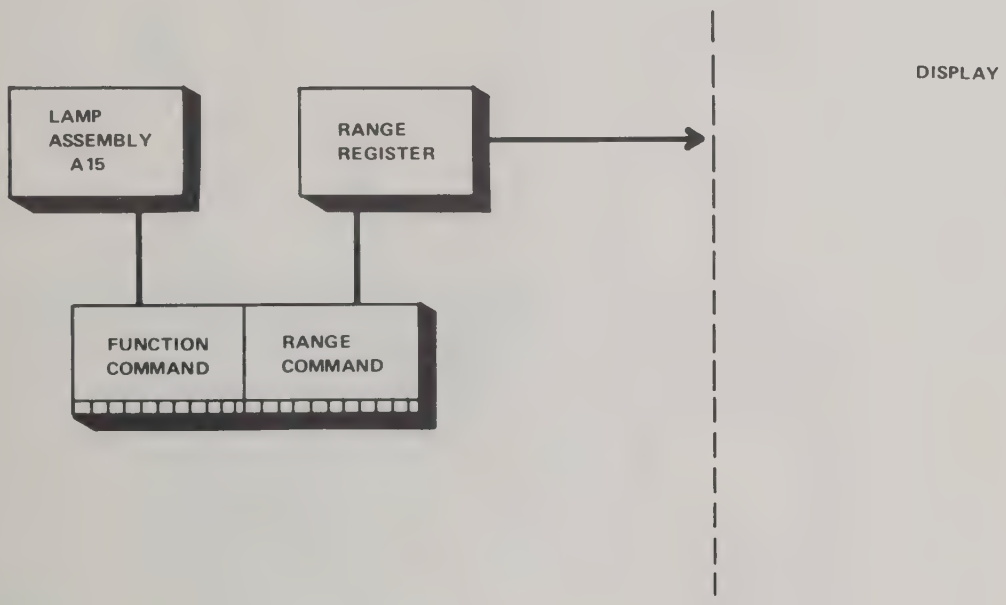


Figure 6. INTERCONNECT (A13)

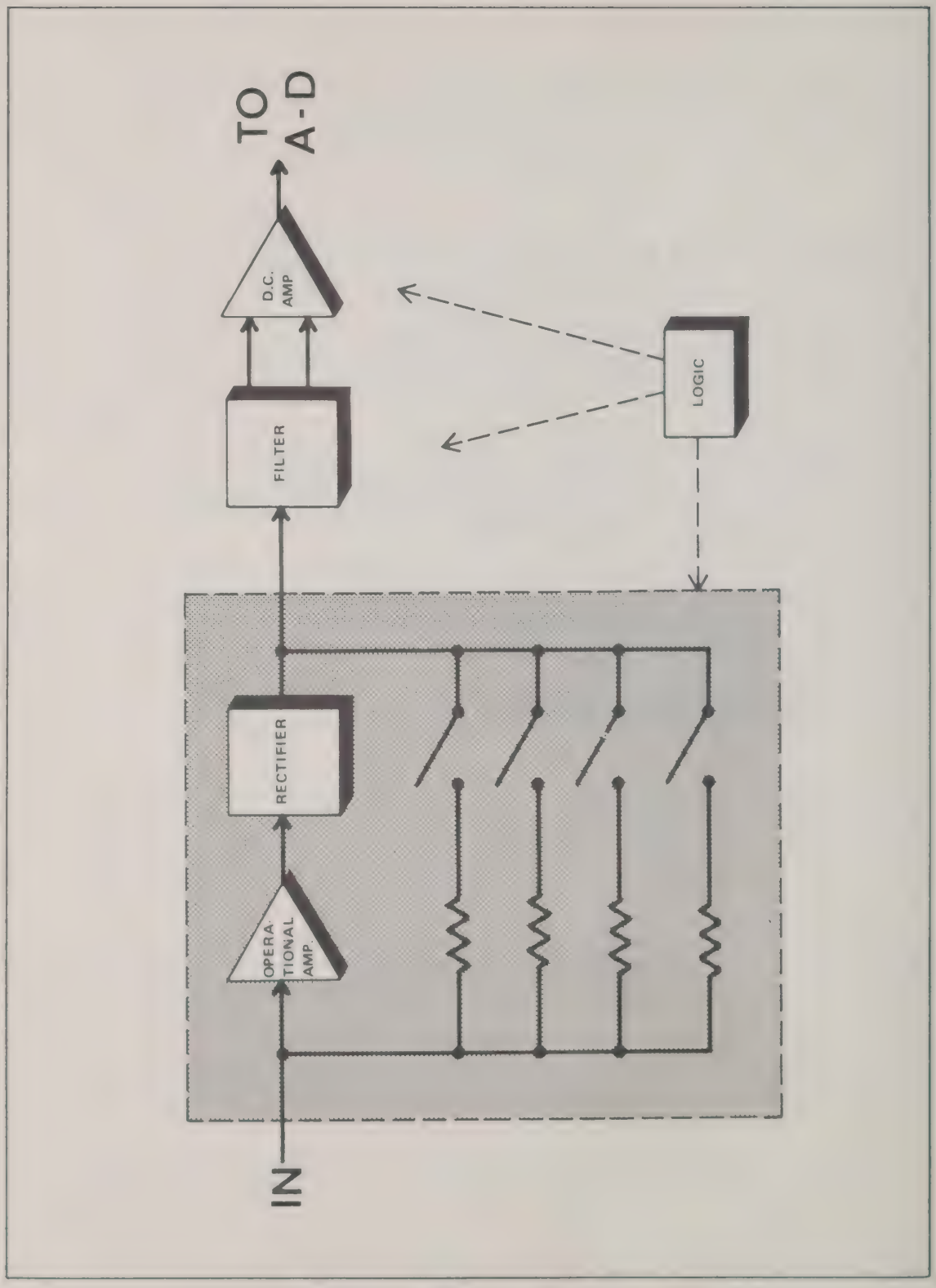


Figure 7. AC CONVERTER –01

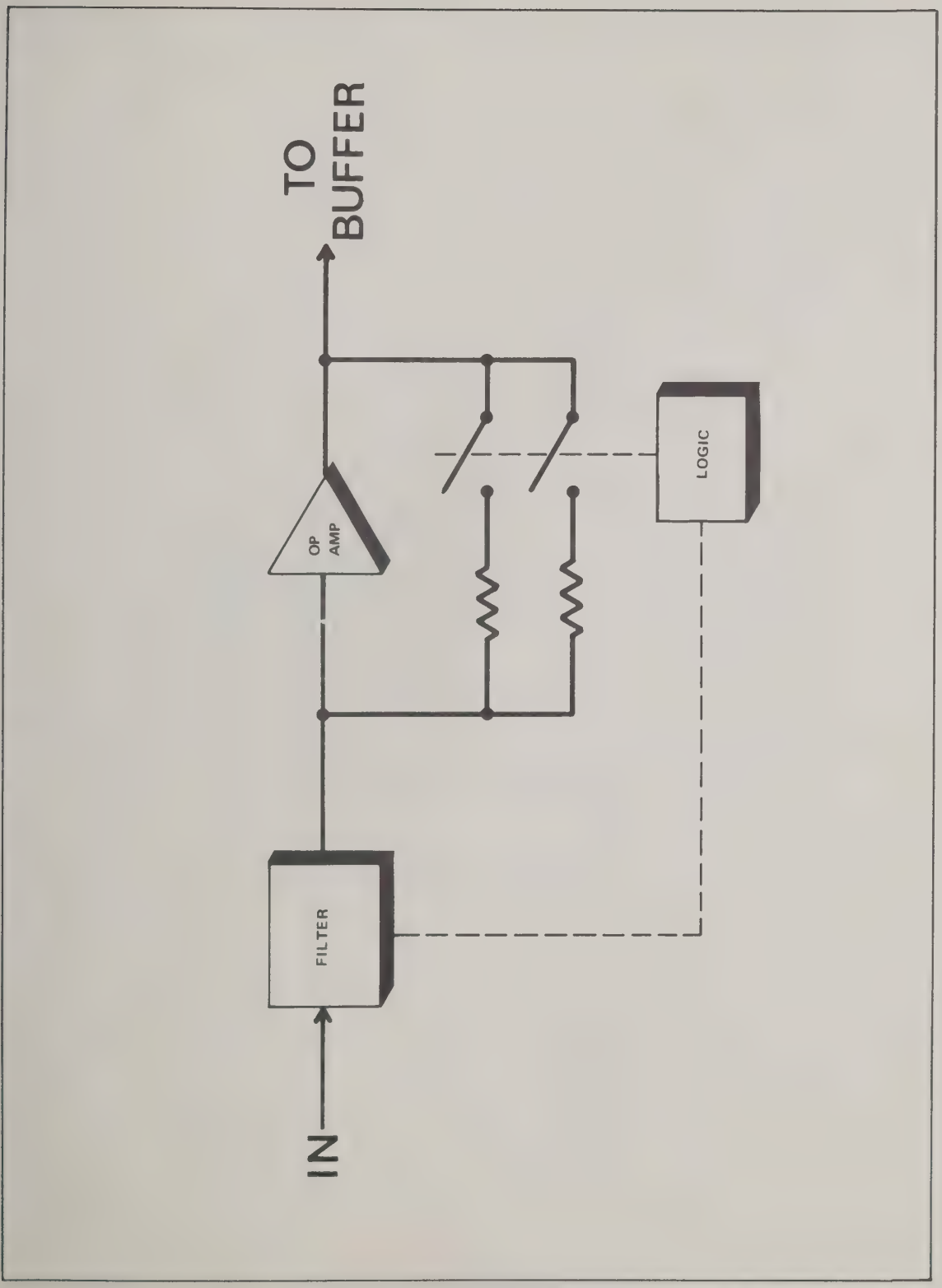


Figure 8. MV CONVERTER –02

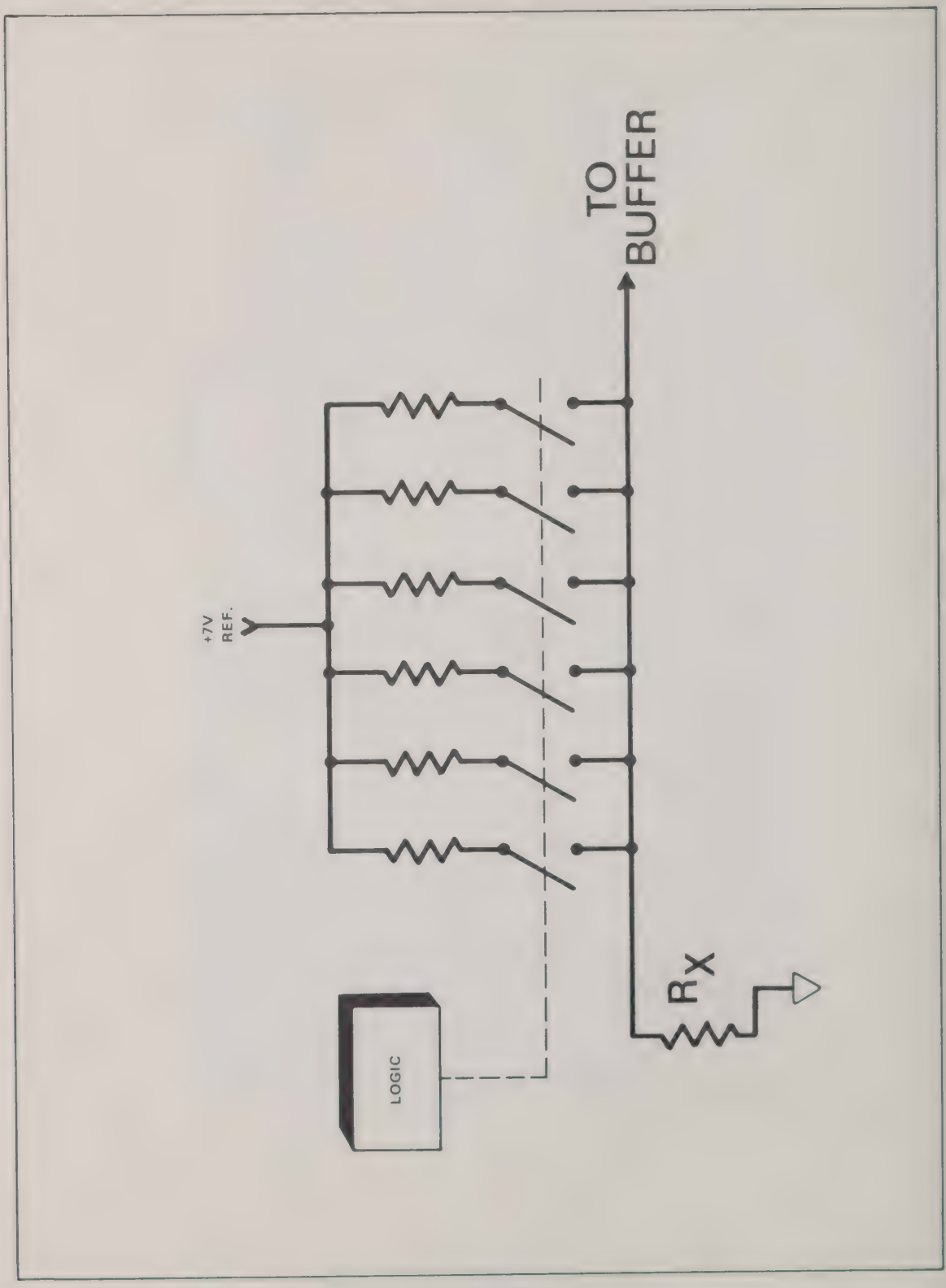


Figure 9. Ω CONVERTER –03

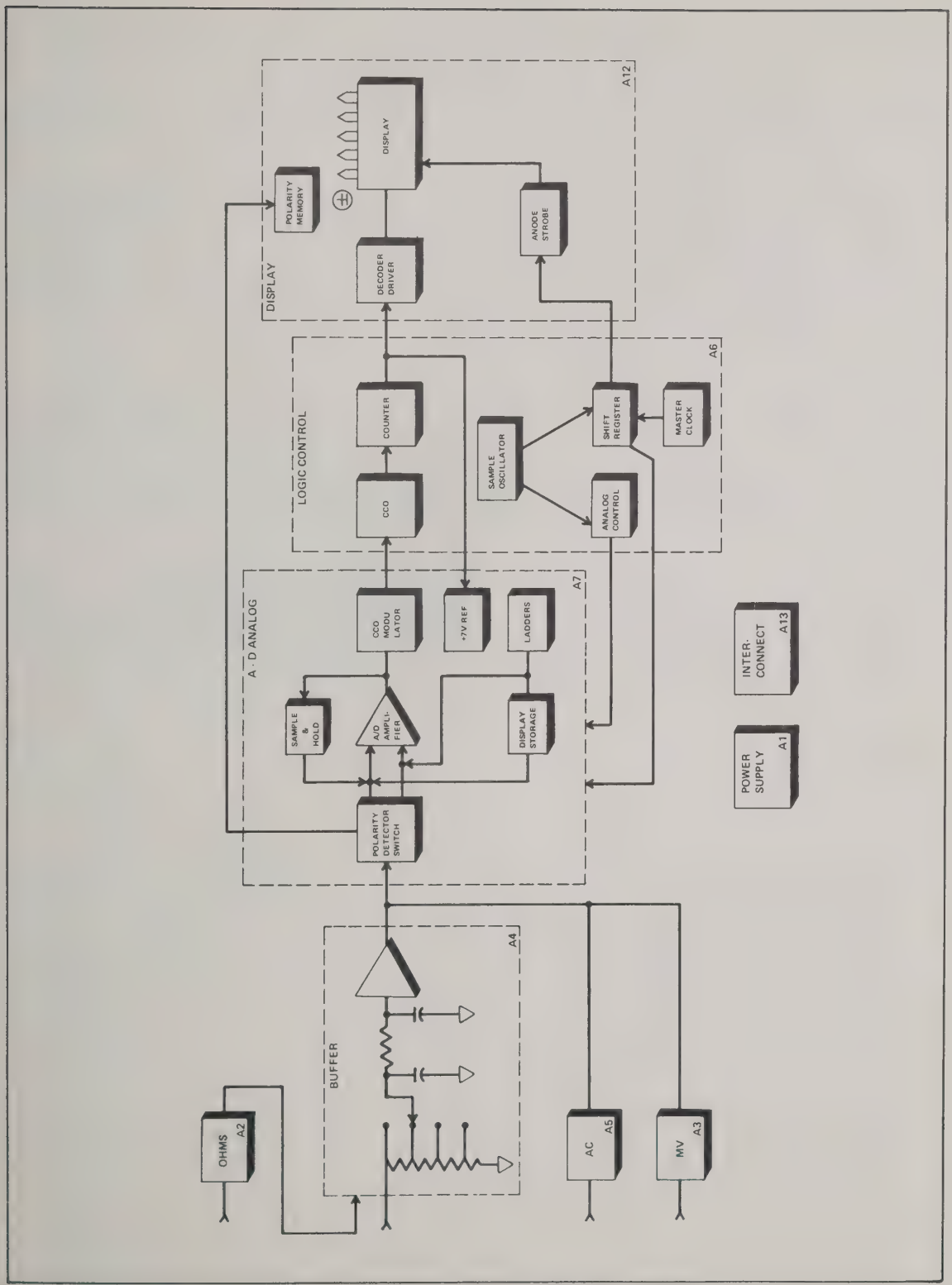


Figure 10. BLOCK DIAGRAM

Note: Since the output of the differential operational amplifier is equal to the difference in input voltage times the gain, the output of the Primary Ladder would cause the output voltage of the A-to-D Amplifier to decrease until it is below 7 volts. When the output of the A-to-D Amplifier is less than 7 volts the CCO Modulator will supply no more current to the Oscillator. The remainder voltage is divided by 7 and is moved into storage in Sample and Hold.

6. The BCD information from the counter being fed to the Decoder Driver translated into decimal format, and as pointed out previously, will cause a ground to occur on the proper numeral line to all of the display tubes. As the count is finished in each time period, the Anode Strobing circuit will cause the proper display tube to light and display the number that has been grounded. The first display tube displays the number digitized in the A time period. The second display tube displays the number digitized in the second or B time period, etc.

7. The output of the A-to-D Amplifier is divided by 7 prior to placing it in Sample and Hold storage. This is the input difference times 10 since the gain of the amplifier is 70, which is divided by 7 before storage. During the second digitizing or B time period, the first remainder is placed on the input of the A-to-D Amplifier, and is digitized and displayed just as was the first digit. Again, the remainder will be stored in another section of Sample and Hold to be used during the third digitizing period. This process is repeated until all four digits have been digitized and displayed.

8. Display Storage functions in such a manner as to receive an analog charge on each of a series of a capacitors representing the digit that was developed in each digitizing period. Though the analog values are stored initially in the Measurement Mode, the output of the Display Storage is used only during the Storage Mode of operation.

THEORY OF OPERATION

TIME

In the Recirculating Remainder system there is an obvious need for time control for Measurement and Storage Modes of operation, in addition to digitizing, display, error removal, and other switching functions that must be carried out in the instrument. Figure 11 is a timing diagram of the time pulses generated in an 8200. The Master Clock output is a 4 kilohertz pulse. This results in one pulse every 250 micro-seconds. Looking at Logic Control schematic (A6), the Master Clock feeds the clock input of the J-K flip-flop U1B, resulting in the F and $\overline{F}$ outputs; a square wave with a 500 micro-second cycle time. Q2, accepting the F signal, produces, at its collector, the $\overline{H}$ signal which is fed to the Shift Register comprising U2A, U2B, U3A, and U3B. Each of the J-K flip-flops in the Switch Register generates one of the digitizing period pulses. The Q output of flip-flop U2A generates the A time output. U2B generates the B time output. U3A generates the C time output. U3B generates the D time output. $\overline{\text{ZERO}}$ is generated by the NAND gate U4B. The inputs to the NAND gate being $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$; when all of these outputs are high, the $\overline{\text{ZERO}}$ pulse is generated. Looking to the right of the schematic diagram, ZERO pulse is generated by the inversion that takes place through Q9. The Sample Oscillator element is CR2, a programmable unijunction transistor which is RC timed and locked in operation with the Master Clock. From the J-K flip-flop U1A, the M or Measure pulse is derived, which is used throughout the instrument for the Measure Mode functions. In the Analog Control circuitry the gate pulses are generated for the various storing and timing functions throughout the instrument.

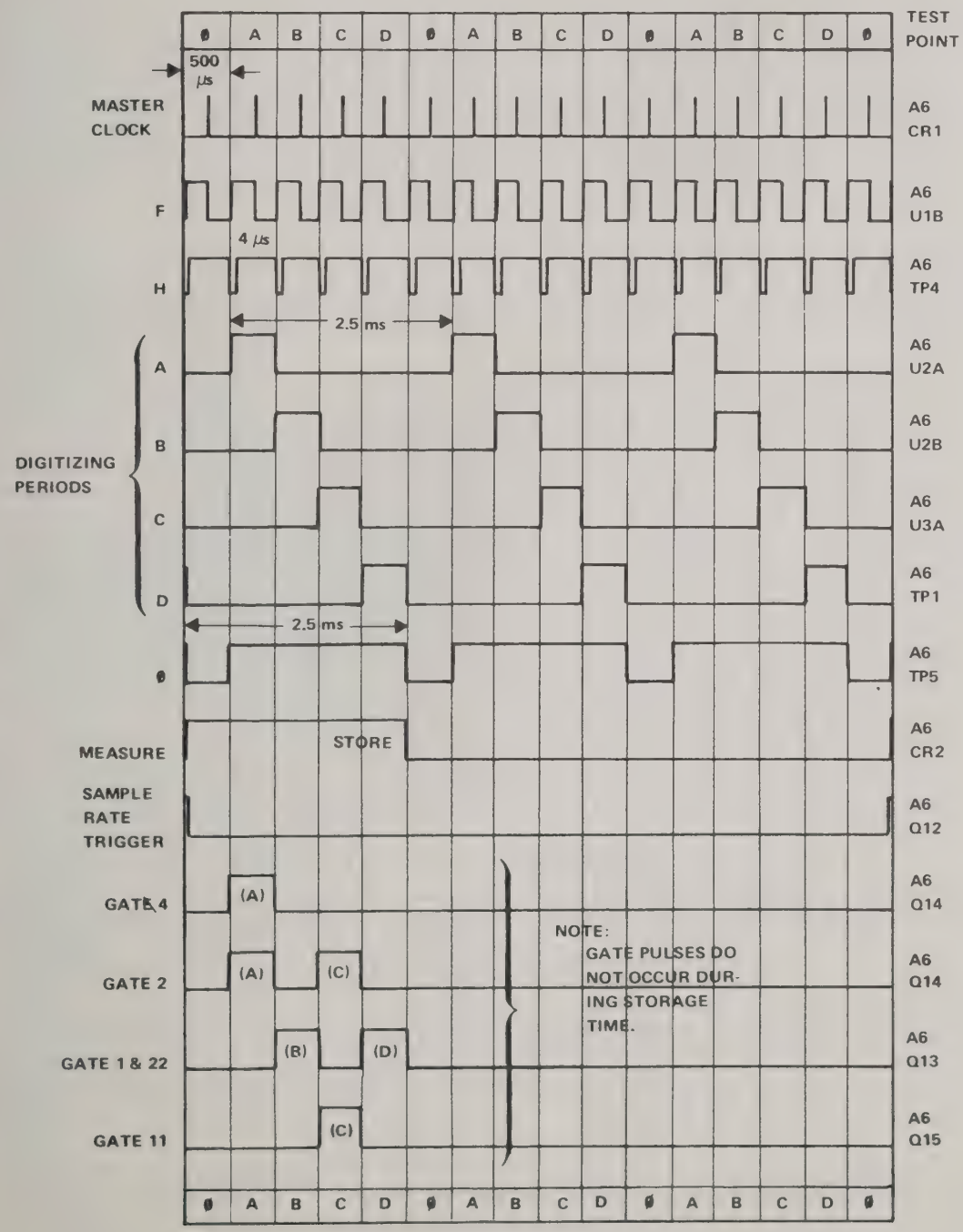


Figure 11. 8200A TIMING DIAGRAM

POWER SUPPLY (A1) Drawing No. 8200A-1001

Voltages from the A17 Transformer assembly are fed to each of three bridge rectifiers. Starting with the regulated +15 volt DC supply, 36 volts AC is applied from the power transformer across the rectifier bridge composed of CR5 through CR8. The positive side of the bridge is fed through R6 and Q3 as the series pass element. It is referenced to the Zener diode CR9. The +15 volt power supply is used as the reference voltage for the other three supplies. Reference for the minus 15 volt supply is developed as a result of the voltage division through R14 and R18 between the plus and minus 15 volt supplies. R21 connects the 5 volt supply back to the 15 volt supply for reference. The 200 volt display supply is connected back from the collector of Q2 to the 15 volt supply; the base of Q2 being connected to the voltage drop between R3 and R4 and is referenced in that manner.

BUFFER (A4) Drawing No. 8200A-1004

The overall gain of the Buffer is 1 inverted, and the Buffer serves five separate functions: an Input Divider, an Active Filter, Overload Protection, the Buffer Amplifier, and the Logic circuitry.

The Input Divider offers an input impedance of 10,000 meg ohms shunted by less than 130 pf, and in the 10 to 1000 volt ranges offers an input impedance of 10 meg ohms. Monolithis amplifier U1 serves as the active element in the filter. K6 closes to activate the filter, which provides 60 db at 50 hertz and 100 db at 200 hertz and above. CR25 and CR26 serve as protection diodes and rapid overload recovery, while CR23 and CR24 protect the filter amplifier.

Overload protection has been provided that operates at a 2 volt level as provided by CR1, CR2, Q6, and Q7. They operate with 1.4 volts on the base and .6 volts on the emitter, and serve to keep U2 and the U3, the Buffer Amplifiers, in linear operation. VS1, a neon bulb, holds the input potential below 100 volts and indirectly illuminates the readout portion of the front panel. CR3 and CR4, at the output of the Buffer Amplifier, serve function as a fast feedback for over voltage,preventing saturation in the amplifier. The amplifier itself being a differential input operational amplifier with a total gain of 1 and composed of dual FET U2 and monolithic amplifier U3.

A-TO-D ANALOG ASSEMBLY (A7) Drawing No. 8200A-1007

Seven separate circuits make up the A-to-D Analog Assembly: the Polarity Detector, A-to-D Amplifier, CCO Modulator, Sample and Hold circuit, Ladder circuit, Display Storage, and +7 volt Reference Supply. The Polarity Circuit consists of three transistors, Q13, Q14, and Q15, which operate the polarity switches consisting of FET's Q10, Q12, and Q16. The Polarity Detector is enabled by the pulse GATE 4 at Q13. GATE 4, consisting of A time, and Measure Mode, is generated in the Logic Control assembly A6. A negative voltage appearing on R15 will cause Q14 to conduct. The line P from the emitter of Q14 will go high, and Q10 and Q16 will conduct. If, in contrast, the voltage on R15 is positive, Q15 will conduct, $\overline{P}$ from the emitter of Q15 will go high and Q12 will turn ON. The voltage on R15 is opposite in polarity to the input of the instrument due to the inversion in the Buffer. The P and $\overline{P}$ signals are used in the Display circuit to indicate polarity. If $\overline{P}$ is high, positive voltage is being fed to the 8200. If P is high, negative voltage is being fed to the 8200.

The A-to-D Amplifier consists of a dual FET, U3, and a monolithic amplifier U2. The overall gain of the amplifier is 70, and its normal input is from zero to 1.6 volts. It is connected as a differential input operational amplifier. Offset removal is accomplished with C7 and FET switches Q16 and Q20. During the ZERO time period Q16 and Q20 conduct placing C7 in the output of the A-to-D Amplifier. When the ZERO pulse is completed, Q16 and Q20 open, C7 is effectively placed in series with the amplifier. Q16 functions to short the input of the A-to-D Amplifier, and Q20 functions to connect C7 to a 1 to 69 divider in the A-to-D Amplifier output. In this manner, offset is removed from the A-to-D Amplifier.

Q19 and Q21 provide a fast feedback circuit to prevent the amplifier from saturating. Such precautions are necessary, in that an operational amplifier once saturated generally takes several seconds to recover. Q11, in the input circuit of the Amplifier, is a temperature compensation device.

The CCO modulator, or constant current oscillator modulator, operates to produce current from the emitters of U26 and U30 to operate the constant current oscillator. When the output of the A-to-D Amplifier is above 7 volts, the modulator is caused to supply current. Q26 supplies the high current during large voltage outputs, and the differential pair Q27 and Q28 control Q29 and Q30 to supply current when the output approaches 7 volts. R48 adjusts the activation point of Q27.

Q22, Q23, Q24, and Q25 are connected to gate pulses that appear only during Measure Mode. In the block diagram explanation it was pointed out that Sample and Hold operates only during the Measure Mode. Capacitor C9 stores the remainder in the A time period. No remainder is stored in the D time period.

The Primary and Secondary Ladders are caused to operate by a single set of Ladder Switches composed of Q31 through Q42. Q39 through Q42 accept the $\overline{W}$, $\overline{X}$, $\overline{Y}$, and $\overline{Z}$ information from the BCD Counter and translate the BCD information into ladder switching. The Primary Ladder is composed of R55, R57, R59, and R61, plus R52 and R53 which serve as calibration resistors. The Secondary Ladder is composed of R54, R56, R58, and R60. In addition, R51 and R74 add one-half digit of bias for the Display Storage to compensate for possible leakage. The output steps of the ladder are in Binary Coded Decimal 8421 format. The output of the Primary Ladder feeds the input of the A-to-D Amplifier. The output of the Secondary Ladder feeds the Display Storage circuitry.

As was covered in the block diagram description, Display Storage is used in Storage Mode only. Display Storage consists of Q4 through Q9. Q4 is enabled by the STORE IN pulse which occurs during the last half of each digitizing period, and provides a path from the Secondary Ladder to the storage capacitors C3 through C6. The analog value representing the numbers that have been digitized are stored in these four capacitors.

The STORAGE OUT pulse on the gate of Q9 occurs only during the Storage Mode.

During Measure Mode analog values are placed in storage, since STORE IN and each of the store A, B, C, and D pulses occur. None of the voltages are taken out during Measure Mode, since the STORAGE OUT pulse on the gate of Q9 does not occur in Measure Mode.

In Storage Mode the STORAGE OUT pulse occurs and connects storage capacitor C3 to the input of the A-to-D Amplifier. After the first digit is digitized the voltage is restored during the last half of the time period by the STORE pulse enabling the gate of Q4. Each increment stored on the capacitors is digitized and the analog value restored on the respective capacitors in a similar manner.

+7 Volt Reference Supply

The +7V Reference Supply is fed power by the +15V Supply and referenced to a zener pack U1. R7, R8, and R9 form a voltage divider for the adjustment of the +7V. R75 protects Q1, the series pass element, from short circuits, and the +7V DISABLE, when grounded, removes the drive of Q1 disabling the +7V reference supply. This is done in order to feed the instrument with External Reference Voltage.

Master Clock

The Master Clock, composed of CR1 and Q1, is an RC control generator operating at approximately 4 kHz, and can be reset by the Data Output option or the Printer Output option producing a pulse on the Master Clock reset line, which connects to the emitter of Q1. The output of the Master Clock is applied to J-K flip-flop U1D. The outputs of U1D carry the F and $\overline{F}$ pulses. Referring to Figure 11, the relationship between Master Clock pulses and the remaining pulses generated in the Logic Control assembly can be seen. The F pulse is applied to the base of U2, and from the emitter of U2 we generate the $\overline{H}$ pulse which is applied to the Shift Register.

Shift Register

Four J-K flip-flops in series U2A, U2B, U3A, and U3B form the Shift Register, which divides the H pulses and produces the four digitizing period time pulses A, B, C, and D. $\overline{ZERO}$ pulse is generated by feeding the outputs of the Shift Register to a NAND gate U4B, and the ZERO pulse is generated by the inversion created by feeding $\overline{ZERO}$ to the base of Q9. The Shift Register may be reset by the Shift Register reset line which is connected to the four flip-flops in the Shift Register and to the set line of U1D.

Sample Oscillator

The Sample Oscillator is a programmable unijunction transistor CR2, which is RC timed by R13 and C3 and operates at a 4 kHz rate. The Sample Oscillator can be keyed by the Sample Oscillator pulse line. The output of the Sample Oscillator is fed to the J input of a J-K flip-flop U1A. The ZERO pulse is connected to the clock input of that same flip-flop. This causes the Measure Pulse or impulse to be generated at the start of ZERO time.

Analog Control

The Analog Control circuits generate the Store A, Store B, Store C, and Store D pulses, which are used in the A-to-D Analog Module. The Shift Register $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$ pulses are connected to the bases of Q5 through Q8. Their emitters are connected back to the Shift Register reset line so the Analog Control Store pulses are disabled during the reset pulse.

Current Controlled Oscillator

The Current Controlled Oscillator, which is the multivibrator formed by Q3 and Q4, receives its current input from the CCO modulator in the A-to-D Analog Assembly, and supplies a pulse train when it receives current. The pulse output is proportional to the current being fed to the multivibrator. The higher the current being fed, the higher the pulse rate. The Current Controlled Oscillator is enabled by the F pulse and held disabled during the $\overline{H}$ time or reset period. This enables the Current Controlled Oscillator during the first half of each digitizing period after the reset pulse is completed.

Counter

Four J-K flip-flops make up the BCD Counter formed by U5A, U5B, U6A, and U6B. The Z, Y, X, and W outputs of the Counter are shown on the 16 state Binary Counter table shown in Figure 12, the Z output representing a binary 1, the Y output a binary 2, the X output a

binary 4, and the W output a binary 8. The NAND gate U4A is the up-ranging element in the system, generating a UP signal when Z, Y, X, and W are all high. The down-range signal is generated by U8B when Z, Y, X, and W are all low. The UP and DOWN signals are fed to the Interconnect assembly where the additional qualifying pulses. Measure and time period A, are added in order to enable autoranging only during the A time period of Measurement Mode.

STORE IN, STORE OUT, and gate pulses are generated in the logic control assembly by the action of Q10 through Q15 and NAND gates U7A, U7B, U7C, and U7D.

DISPLAY (A12) Drawing No. 8200A-1012

Numbers are displayed in sequence. The A time period displays the most significant digit. The B time period displays the second most significant digit, etc. until all four digits have been displayed. The A digit includes over-ranging to 15 and each digit is displayed only during the last half of its respective time period. During the ZERO time period none of the display tubes are on.

Anode Strobing

Looking at display assembly schematic A12, when the F signal is low, which occurs during the last of each digitizing period, it enables transistors Q5, through Q8, which completes one-half of the ON path for each of those transistors. The other half of the ON signal for those transistors consists of the digitizing pulses applied to their bases. For example, the digitizing A pulse being applied to the base of Q5 will turn Q5 ON during the A time period when F is low. This occurs during the last half of the A time period and Q5 will conduct causing Q1 to conduct and apply the 200 volt ionizing voltage to the anode of DS3 which will cause any number to ionize which has been grounded by U1, the Decoder Driver.

Polarity Memory

CR6 and CR7 operate as a NOR gate. If VDC or MV are selected the VDC CONTROL or MV CONTROL line will go low enabling Q13 and Q14. The P and the $\overline{P}$ signal lines carry the polarity information from the A-to-D amplifier assembly detector. If P is high a negative voltage is being fed into the 8200A. If $\overline{P}$ goes high a positive voltage is fed into the instrument. The signals P and $\overline{P}$ last only during the A time period of Measurement Mode. The P signal will turn on the gate of Q15 causing it to conduct and causing the multivibrator, formed by Q13 and Q14, to flop to a condition wherein the potential on the collector of Q13 will cause a low voltage on the minus sign in DS1 which will be pulsed on during the B time period when Q6 has turned on by the base signal on its base and the F signal on it's emitter. This conduction will cause Q18 to conduct and allow the 200 volts to be applied to V1. The polarity memory circuit is a flip-flop formed by Q13 and Q14 that remains in which ever state it was pulsed to last.

Decoder Driver

Decoder Driver U1 translates the BCD coded information on the W, X, Y, and Z lines which are inverted by inverters U2A, U2D, U2E, and U2F into grounds on the appropriate lines to all the display tubes. It should be noted that this is a 16 state Counter and care should be taken if any attempt is made to substitute this decoder driver, in that most decoder drivers count to 9 or 10, consequently substitution can lead to problems in the 8200.

Lamp Assembly

A small printed circuit board mounted on the display assembly contains the POWER, REMOTE, EXT REF, and FILTER switches plus two indicator lamps indicating filter selection and external reference selection. This assembly also carries the Millivolt ZERO potentiometer which is connected between +5 and −15 volts and is mounted on this board so that it may be adjusted via a hole in the front panel.

INTERCONNECT (A13) Drawing No. 8200A-1013

Function Command

When the 8200 is in local control a ground is furnished on J12 Pin 30 which is series connected through all six function switches. In addition, the function switches are mechanically interlocked to prevent operation of more than one switch at a time. If the REMOTE switch is operated no ground is furnished to pin 30 and the functions will be controlled from the Remote Control Assembly (A8).

Range Command

A ground signal is series connected through the Range Command switches which supply the $\overline{Ra}$, $\overline{Rb}$, $\overline{Sa}$, and $\overline{Sb}$ lines which control the Range Register.

Range Register

U1A and U1B are J-K flip-flops with outputs of a, $\overline{a}$, b, and $\overline{b}$, the range control signals. Range code is given in Figure 12. These range code signals are generated when the instrument is in both manual and autoranging and are fed to each input circuit to control the relays in that circuit.

As was pointed out in the Logic section $\overline{UP}$ and DN signals are generated when the count from the BCD counter reached 15 for a $\overline{UP}$ signal or was ZERO to generate a DN or down signal. These signals being fed to the Range Register through additional signal qualifiers will only cause a range change when the clock input to U1B or U1A, the $\overline{MaF}$ signal, is available which occurs only during Measurement mode in the A time period when the F signal is high. So ranging can occur only in Measurement mode in the A time period.

MILLIVOLT CONVERTER −02 OPTION (A3) Drawing No. 8200A-1003

The Millivolt Converter consists of an operational amplifier with a dual gain of 10 or 100 and feeds the A/D Analog assembly in the 8200. This makes possible ranges of 100 millivolts and 10 millivolts. The output range of the Millivolt Converter is ZERO to 1.6 volts and it contains A3 pole filter. The input of this amplifier consists of a dual transistor U7 which gives excellent temperature and bias characteristics in addition to a very low noise input. The Millivolt Converter also contains its own logic for autoranging, including the DC ranges. U6 is a monolithic operational amplifier with both low bias and low drift and whose output drives Q5 or Q6 to provide polarity spreading in the output and increase the current drive.

K1 closes whenever the millivolt function is selected. This connects the high terminal to the amplifier and provides a connection for the low terminal to signal common. K3 selects the output range of the instrument. With K3 closed the instrument is in the 100 millivolt range as determined by the feedback resistance. The Millivolt ZERO is adjusted by R15 which can be adjusted through

an access hole in the front panel of the instrument when the Millivolt Converter is installed. R13 adjusts the millivolt bias current.

Overload protection is provided by CR1, CR2, CR3, and CR4. Current can be conducted through CR1 or CR2 and through R28 or R29 back to the LOW terminal in overload conditions. Similarly, current may be conducted through R3, R4, CR3, CR4, and R19. The output of the amplifier is limited by R20 and R21. These resistors limit the maximum current available to R23.

When the millivolt option is installed, the MV SENSE RANGE line is automatically connected to logic common. This defeats the VDC control command on the Buffer board. The new VDC control and MVDC control are both on the millivolt board. There is a 2 state flip-flop comprised of U4A and U4D which selects either the millivolt or the volt DC range when either the $\overline{\text{MVDC}}$ CONTROL or $\overline{\text{VDC}}$ CONTROL is low. The autorange and logic is provided by U1A, U2C, U3B, and U3A. When the Millivolt Converter is installed, the function lights associated with the Millivolt Converter operate, in that all of the interconnect wiring is already accomplished in the basic instrument.

AC CONVERTER –01 OPTION (A5) Drawing No. 8200A-1005

The AC Converter is composed of two basic circuits plus logic. An operational rectifier which is composed of Q1, a voltage follower used to reduce the capacitance and increase the input impedance, Q3 and Q4 a differential pair for current supply, Q2 and Q5 which supply the bias current to make the clipping symmetrical, and Q6 which compensates for the diode capacity while CR7 and CR8 provide protection for Q3 and Q4. Feedback switching is used in the amplifier to accomplish range switching.

The operational rectifier is followed by a DC difference amplifier with about 2 ma of output at full-scale. It includes RC filtering and spreading diodes CR13 and CR14 to enhance the polarity signal. U3 is a monolethic operational amplifier that has been selected for its low drift characteristics.

$\overline{\text{VAC}}$ CONTROL line will activate K1 and K2. Range code information into U1A, U1B, U1C, and U1D provide the necessary drive signals for K3, K4, and K5, the ranging relays.

The input is capacitively coupled through C1 to R1 and C2 in parallel combination. Q1 is a voltage following amplifier whose function is to reduce the input capacity and increase the input resistance of the amplifier. Q2 is a differential amplifier with one input capacitively coupled to Q1 while the other input is coupled to ground. The output of this differential amplifier is applied to the differential pair Q3 and Q4. Q2 biases this differential pair. Q5 is used to bias the differential amplifier U2 and control the level of the collector of Q4. The level determines the symmetry of the circuit. R31 is the symmetry control. CR11 and CR12 in conjunction with the amplifier operate as an operational rectifier. The output of these two diodes is passed through a DC difference amplifier integrator. The output of these diodes is roughly divided by 10 either by R34, R35, or R36 and R35 which forms the output voltage dividers. The signal on R35 is then fed back through the range determining feedback resistors to the summing junction which is the gate of Q1. R16 and R23 constitute the resistive feedback for the 1 volt range. R17 and R24 constitute the resistive feedback for the 10 volt range. R18 and R25 are the feedback circuit for the 100 volt range and R19 is used as the feedback resistor for the 1000 volt range. Feedback capacity for the 1 volt range is composed of C11 while C12 and C15 serve the same function for the 10 volt range and C13, C16, and C17 form the capacity feedback for the 100 volt range and C18 is the feedback capacity for the 1000 volt range. These capacitors compensate for the capacity of C2 in the input.

The DC difference amplifier takes the difference between the positive and negative signal, rectifies sign waves, averages them, and produces a DC output. Spreading diodes CR13 and CR14 serve as a convenience for the polarity sensing to insure the proper polarity into the A-to-D amplifier.

ZERO control is provided by R48 and the associated circuitry of R47 and R44. U3 is a selected low drive amplifier with an overall gain such that a 1 volt peak sign wave input will result in .707 volts of output. Thus, the output represents the RMS voltage. However, it is average responding. Adjustment of the overall gain is accomplished with R46, then each range is adjusted in sequence. Adjustment and calibration order is given on the inner guard cover on the instrument which must be in place when the instrument is calibrated.

Ohms Converter —03 Option

The Ohms Converter operates in such a manner as to use the 7 volt reference as the source of current flow through the unknown resistance to be measured. The 8200 then measures the voltage drop across the resistor thus providing a direct measure of the voltage across the resistor with a known current. The 10 MΩ range is activated through dividers R1, R2, and R3 in combination with R5, R1 being the calibration adjustment. The divider reduces the voltage on R5 to only .7 of a volt. This eliminates having to have a 70 megohm resistor from the 7 volt supply directly to the INPUT HI.

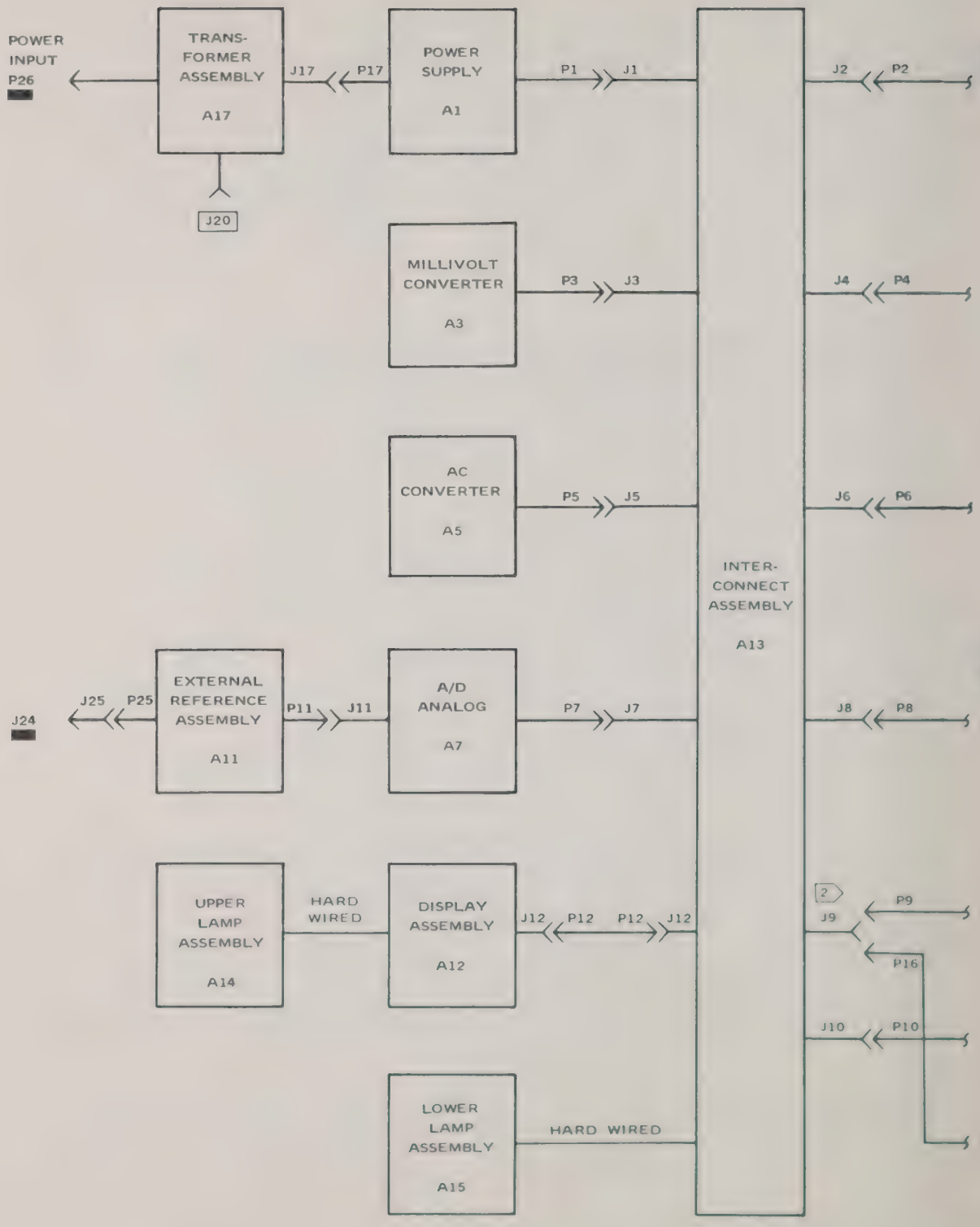
The 1,000 KΩ range is called when K1 is closed. This puts 7 volts across R5 increasing the current from 100 picoamps which was used in the 10 MΩ range to 1 microamp. R4 is the calibration adjustment to this range. The 100 KΩ range is called when both K1 and K2 are operated. R6 and R7 provide an additional 9 microamps making the total current 10 microamps. R6 is the calibration adjustment for this range. The 10 KΩ range is called when K3 is operated. R8 and R9 provide 100 microamps through the resistance to be measured. K8 being the calibration adjustment. The 1 KΩ range is called by operating K3 and K4. R10, R11, and R27 provide an additional 900 microamps or a total of 1 milliamp through the unknown resistance. R10 is the calibration adjustment for the 1 KΩ range. The 100 ohm range is called by operating K5. R12, R13 and R15 provide 10 milliamps of current through the unknown resistor. R12 being the calibration adjustment.

F1 is a fusible link with a current capacity of 100 milliamps. It is activated whenever an overload voltage of greater than 30 volts is applied between HIGH and LOW; CR1 and CR2 together with CR20 and CR21 constitute overload protection dials. CR1 and CR2 are 10 volt zeners while CR20 and CR21 furnish a return path current to INPUT LOW. When excessive voltage is applied to INPUT HIGH, current will flow through range resistors and CR2 or through R14 and CR1. This prevents the input voltage from overpowering the 7 volt supply and destroying parts of the A-to-D Analog circuitry. If voltage greater than 130 volts is applied to the KΩ range, R11 will overheat and possibly be destroyed. No damage will result in the A-to-D Analog assembly.

An Ohms function can be commanded by the $\overline{\Omega}$, $\overline{K\Omega}$ or $\overline{M\Omega}$ CONTROL lines which drive Q3, Q4 or Q5. When the $\overline{AR}$ line is high indicating that a valid range has been called, either Q3, Q4, or Q5 will be ON depending upon which control line is low. The collectors of these transistors are connected through diodes CR13, CR14, and CR15 to reset lines of 3 state flip-flop comprised of U5B, U3A, and U3B.

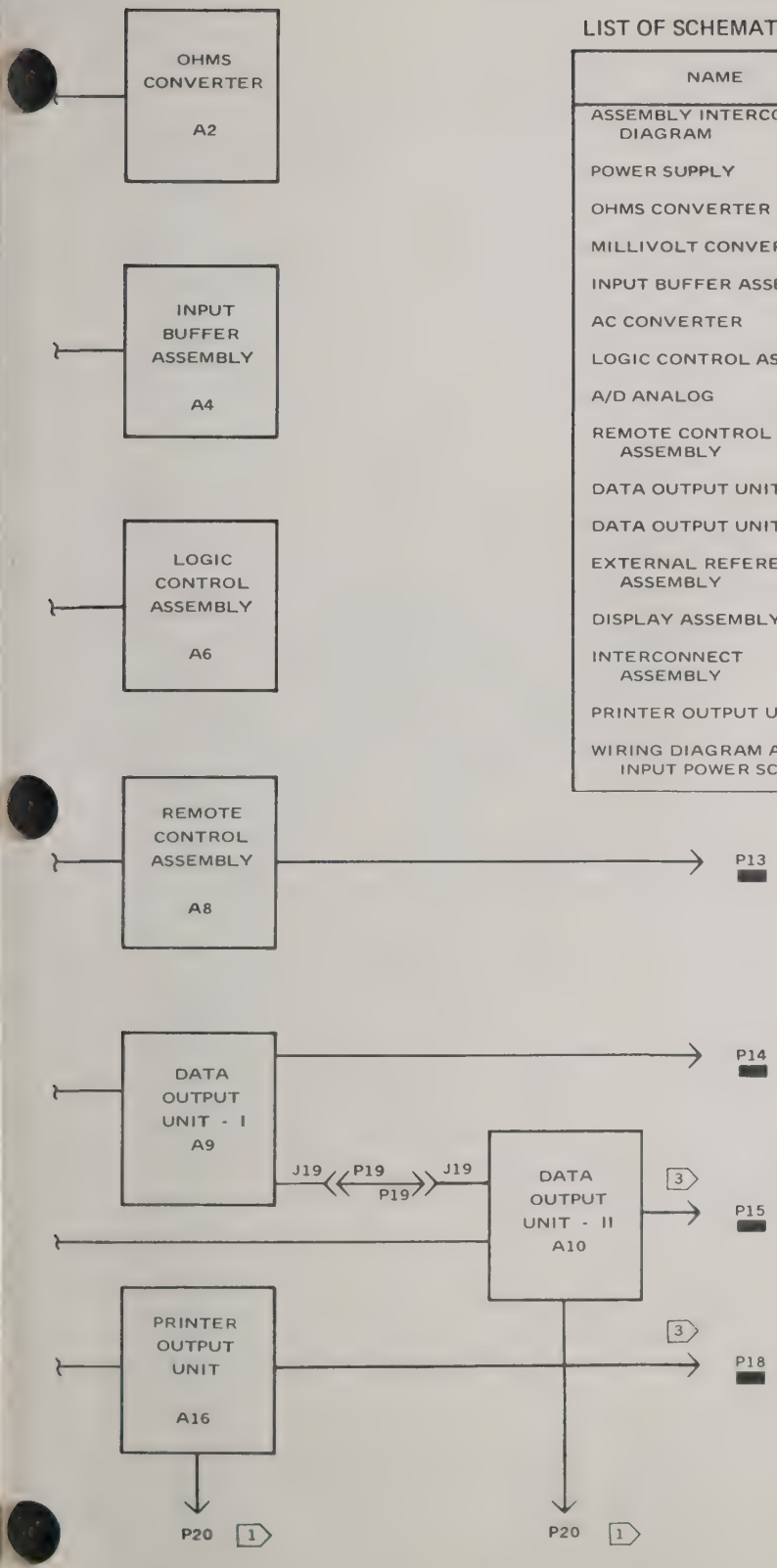
Transistors Q3 through A5 and Q8 through Q10 plus NAND gates U3A, U3B, and U5A combine to command the required functions. NAND gates U4A through U4D plus transistors Q6 and Q7 control the range in the KΩ function. NAND gates U1A, U1B, U2A, and

U2B provide the autoranging gate signals. NAND gate U2D provides a delayed MΩ relay line for the autorange logic on the A13, Interconnect assembly. NAND gate U2C provides a delayed $\overline{\text{OHM}}$ relay line for logic on the Interconnect assembly. The Ohms Converter Option is the only input option that feeds the 8200 Buffer assembly. All other input options feed directly to the A-to-D Analog assembly.


POWER INPUT
P26
TRANS-FORMER ASSEMBLY
A17
J17
P17
POWER SUPPLY
A1
P1
J1
J2
P2
J20
MILLIVOLT CONVERTER
A3
P3
J3
J4
P4
AC CONVERTER
A5
P5
J5
J6
P6
INTER-CONNECT ASSEMBLY
A13
J24
J25
P25
EXTERNAL REFERENCE ASSEMBLY
A11
P11
J11
A/D ANALOG
A7
P7
J7
J8
P8
UPPER LAMP ASSEMBLY
A14
HARD WIRED
DISPLAY ASSEMBLY
A12
J12
P12
P12
J12
2
J9
P9
P16
J10
P10
LOWER LAMP ASSEMBLY
A15
HARD WIRED

LIST OF SCHEMATICS AND DIAGRAMS

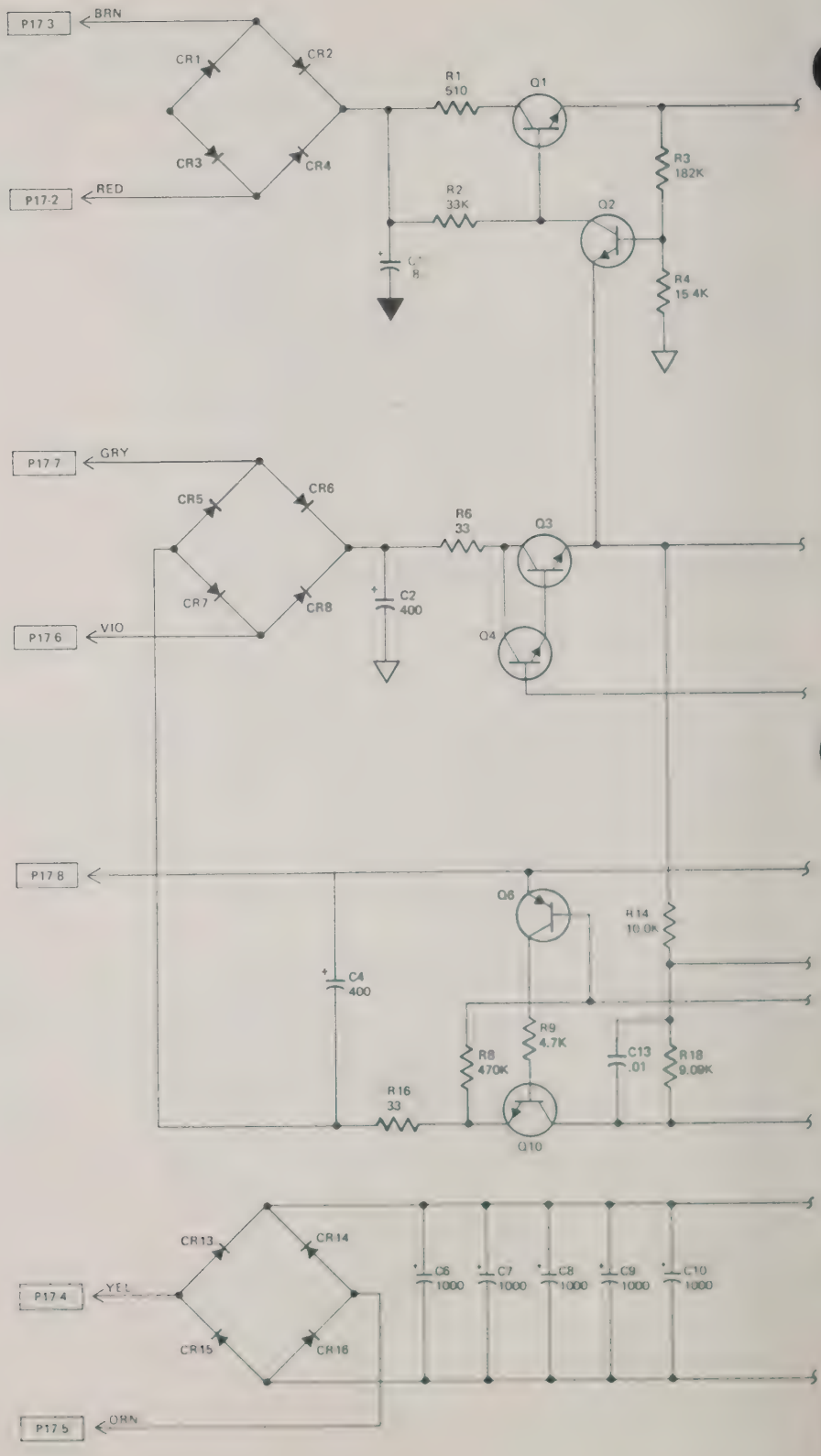
NAME	ASSY. NO.	SCHEM. NO.
ASSEMBLY INTERCONNECT DIAGRAM	NONE	1
POWER SUPPLY	A1	2
OHMS CONVERTER	A2	3
MILLIVOLT CONVERTER	A3	4
INPUT BUFFER ASSEMBLY	A4	5
AC CONVERTER	A5	6
LOGIC CONTROL ASSEMBLY	A6	7
A/D ANALOG	A7	8
REMOTE CONTROL ASSEMBLY	A8	9
DATA OUTPUT UNIT — I	A9	10
DATA OUTPUT UNIT — II	A10	11
EXTERNAL REFERENCE ASSEMBLY	A11	12
DISPLAY ASSEMBLY	A12	13
INTERCONNECT ASSEMBLY	A13	14
PRINTER OUTPUT UNIT	A16	15
WIRING DIAGRAM AND INPUT POWER SCHEMATIC	NONE	16

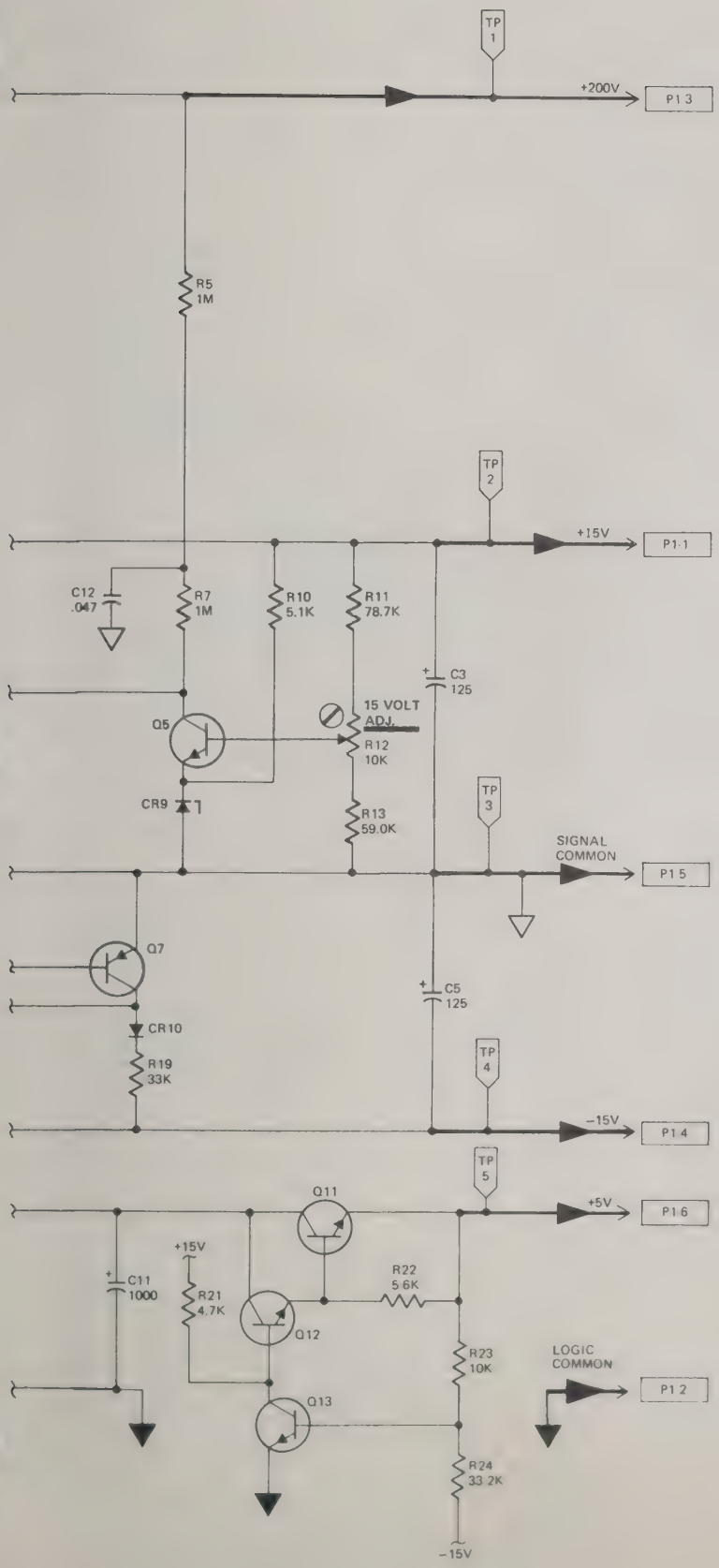


NOTES:

1. ▬ DENOTES REAR PANEL CONNECTOR.
2. [1] MATES WITH A17J20 for +5V LOGIC SUPPLY INPUT POWER: CONNECTIONS FOR ONE ASSEMBLY ONLY, EITHER A10 OR A16.
3. [2] EITHER A9P9 A16P16 MATES WITH J9, SINCE DOU AND POU OPTIONS ARE MUTUALLY EXCLUSIVE.
4. [3] P18 and P15 SHARE THE SAME REAR PANEL LOCATION.

FUNCTIONAL SCHEMATIC DIAGRAM	
1	
ASSEMBLY INTERCONNECT	
Drawing No. 8200A-1100	REV —
FLUKE JOHN FLUKE MFG CO., INC. P.O. Box 7428 Seattle Washington 98133	

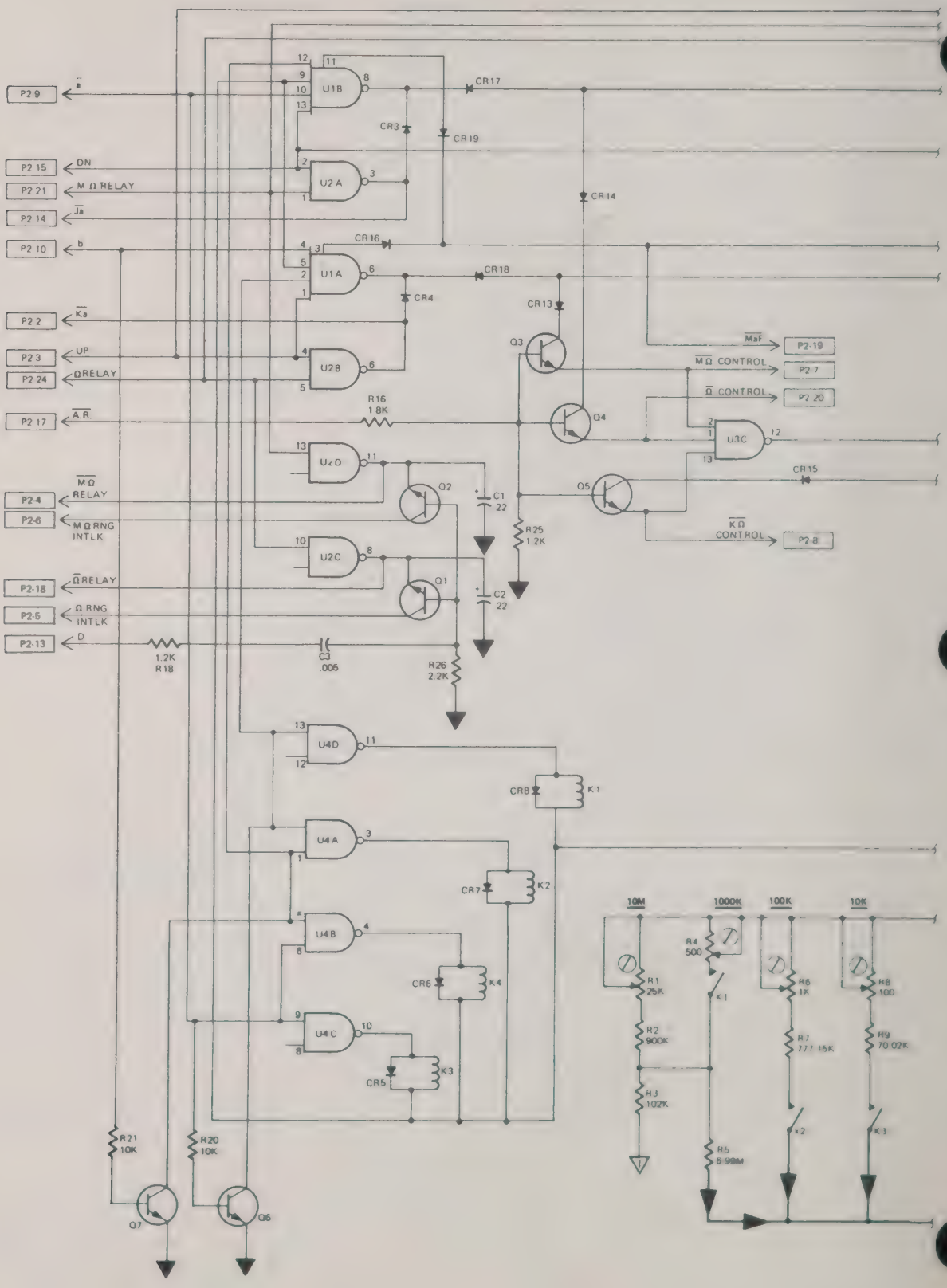

P17 3
BRN
CR1
CR2
CR3
CR4
P17-2
RED
R1
510
Q1
R2
33K
Q2
R3
182K
R4
15.4K
P17 7
GRY
CR5
CR6
CR7
CR8
P17 6
VIO
R6
33
Q3
C2
400
Q4
P17 8
Q6
R14
10.0K
C4
400
R9
4.7K
R8
470K
C13
.01
R18
9.09K
R16
33
Q10
CR13
CR14
P17 4
YEL
CR15
CR16
P17 5
ORN
C6
1000
C7
1000
C8
1000
C9
1000
C10
1000

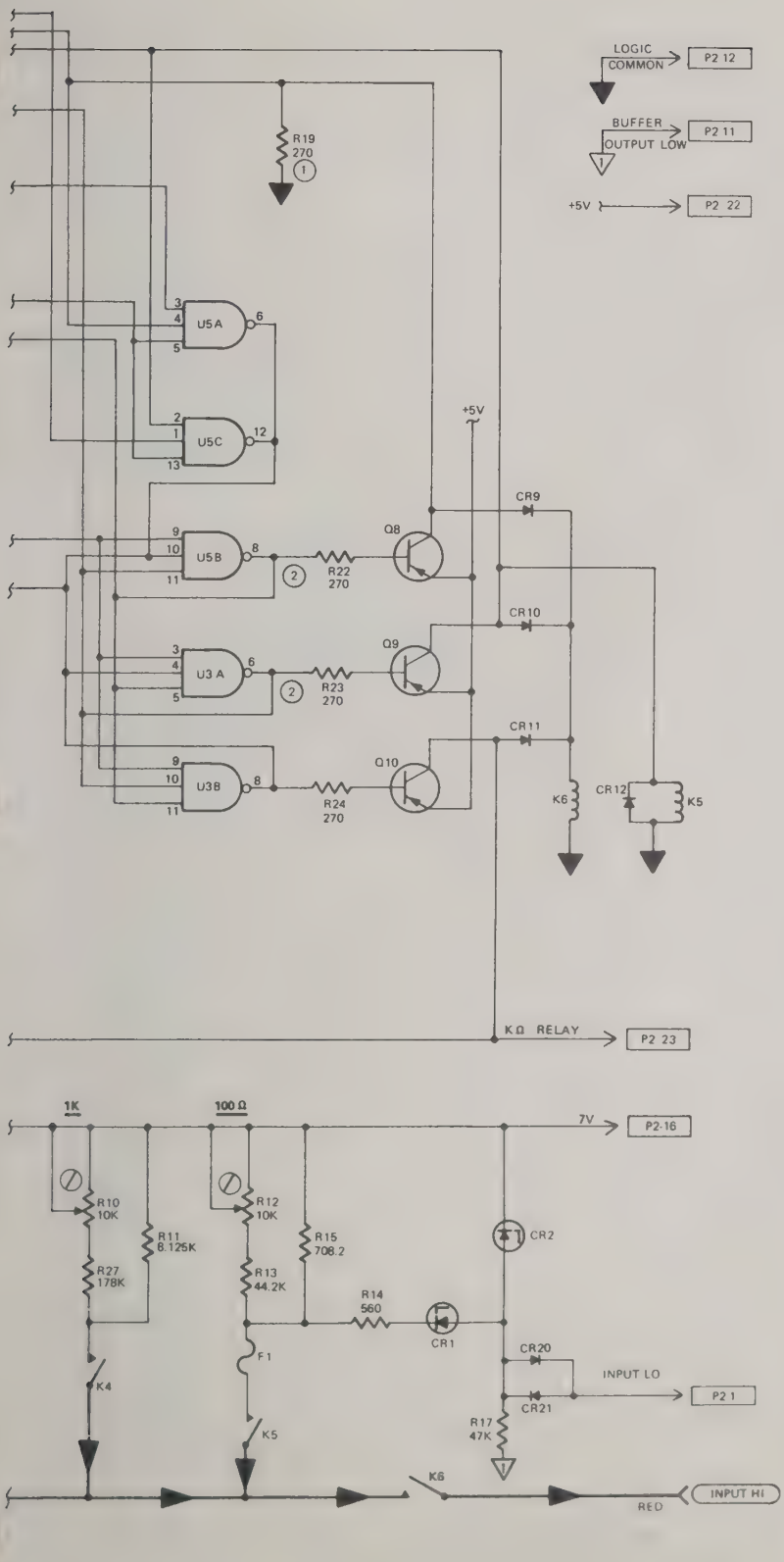


NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⊘ DENOTES INTERNAL ADJUSTMENT.
3. ▼ DENOTES LOGIC COMMON.
4. ▽ DENOTES SIGNAL COMMON.
5. ——▶ DENOTES PRIMARY SIGNAL PATH.

FUNCTIONAL SCHEMATIC DIAGRAM	
A1 POWER SUPPLY	2
Drawing No. 8200A-1001	Rev. a
FLUKE JOHN FLUKE MFG CO., INC P.O. Box 7428 Seattle Washington 98133	


P2 9
P2 15
DN
P2 21
MΩ RELAY
P2 14
P2 10
b
P2 2
P2 3
UP
P2 24
ΩRELAY
P2 17
A.R.
P2-4
MΩ RELAY
P2-6
MΩ RNG INTLK
P2-18
ΩRELAY
P2-5
Ω RNG INTLK
P2-13
D
1.2K R18
R16 18K
C3 .006
R26 2.2K
R25 1.2K
C1 22
C2 22
U1B
U2A
U1A
U2B
U4D
U2C
U3C
U4A
U4B
U4C
CR17
CR19
CR14
CR16
CR18
CR4
CR3
CR13
CR15
CR8
CR7
CR6
CR5
K1
K2
K3
K4
Q1
Q2
Q3
Q4
Q5
Q6
Q7
MaF
MΩ CONTROL
Ω CONTROL
KΩ CONTROL
P2-19
P2 7
P2 20
P2-8
R21 10K
R20 10K
10M
1000K
100K
10K
R1 25K
R2 900K
R3 102K
R4 500
R5 6.99M
R6 1K
R7 777.15K
R8 100
R9 70.02K



IC	PIN CONNECTIONS	
	+5V	COMMON
U1-U5	14	7

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. DENOTES INTERNAL ADJUSTMENT.
3. DENOTES LOGIC COMMON.
4. DENOTES BUFFER OUTPUT LOW.
5. DENOTES FRONT PANEL LOCATION.
6. DENOTES PRIMARY SIGNAL PATH.

CHANGES

(1) R19 ADDED IN SER. NO. 249 AND ON.

(2) R22, R23 CHANGED FROM 390Ω IN SER NO 398 AND ON.

FUNCTIONAL SCHEMATIC DIAGRAM

3

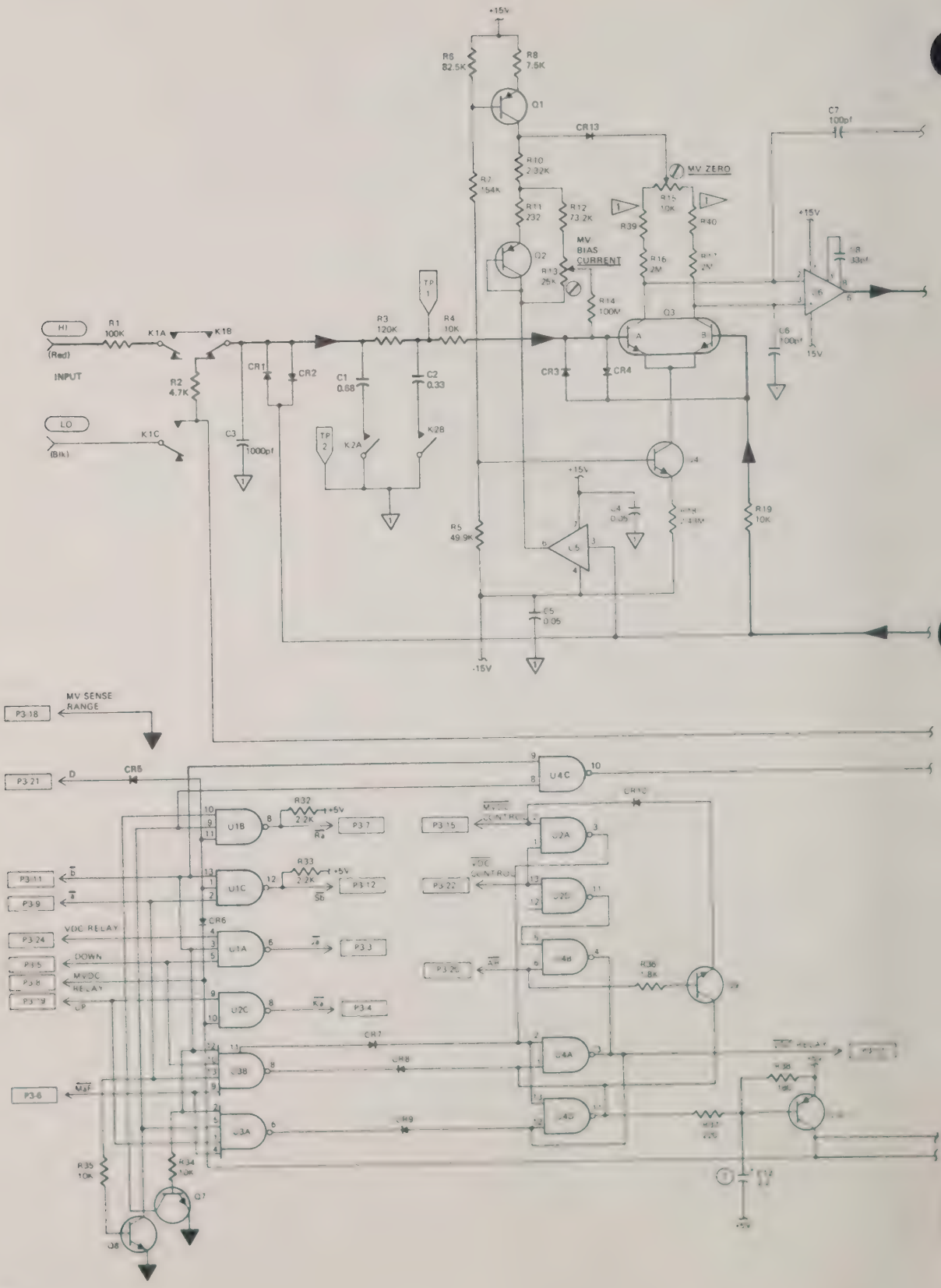
A2

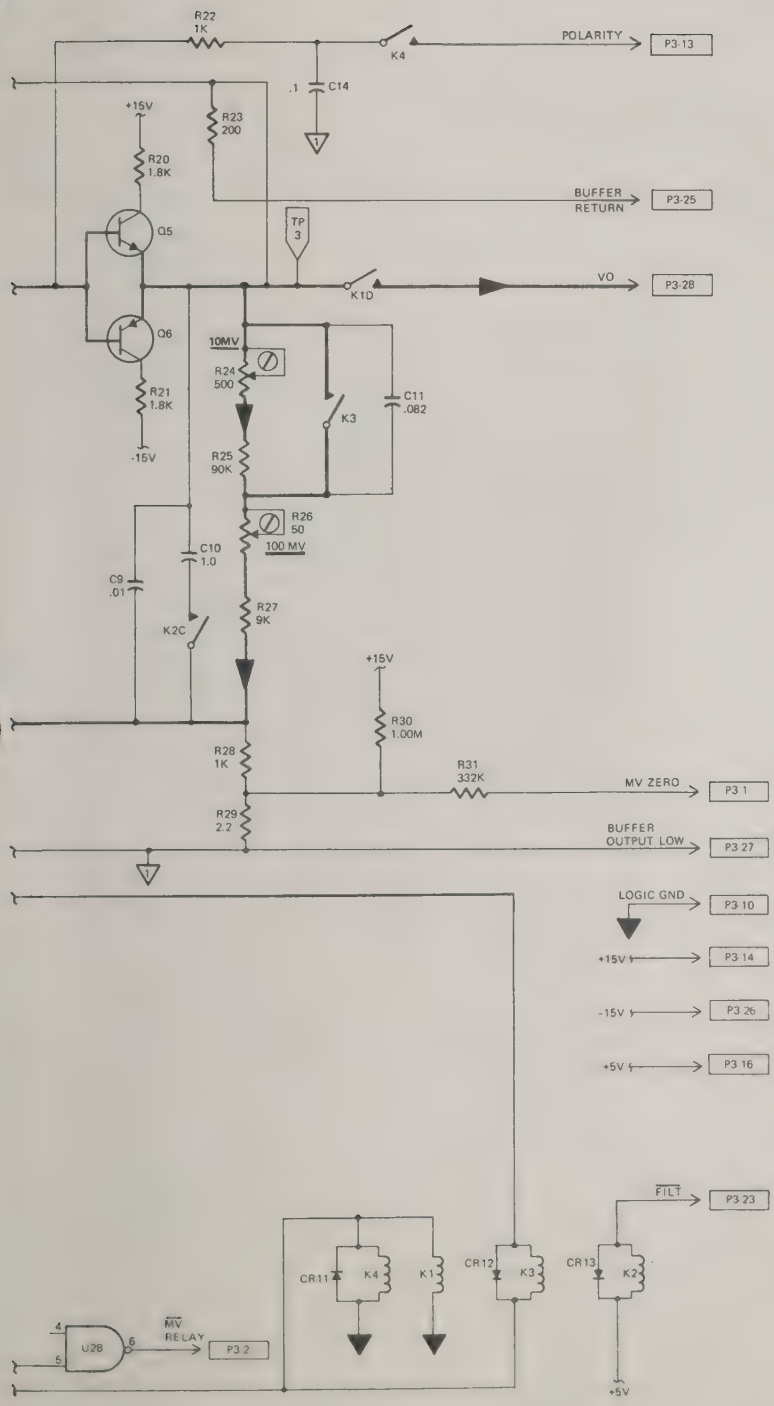
OHMS CONVERTER

Drawing No. 8200A-1002

REV —

FLUKE JOHN FLUKE MFG. CO., INC.
P O Box 7428 Seattle Washington 98133


+15V
R6 82.5K
R8 7.5K
Q1
CR13
C7 100pf
R10 2.32K
R7 154K
MV ZERO
R15 10K
R11 232
R12 73.2K
R39
R40
MV BIAS CURRENT
R13 25K
R16 2M
R14 100M
Q2
Q3
TP 1
HI
R1 100K
K1A
K1B
(Red)
INPUT
R2 4.7K
CR1
CR2
C1 0.68
C2 0.33
R3 120K
R4 10K
CR3
CR4
LO
K1C
(Blk)
C3 1000pf
TP 2
K2A
K2B
C5 0.05
R5 49.9K
R19 10K
-15V
MV SENSE RANGE
P3-18
P3-21
D
CR5
U4C
U1B
R32 2.2K
P3-7
P3-11
P3-9
U1C
R33 2.2K
P3-12
CR6
VDC RELAY
P3-24
P3-5
DOWN
P3-6
MV/DC RELAY
P3-8
UP
U1A
U2C
P3-3
P3-4
CR7
CR8
CR9
U3B
U3A
P3-6
R35 10K
R34 10K
Q7
U2A
U2B
P3-15
P3-22
P3-2
R36 1.8K
U4A
U4D
R38 10K
C8 33pf
U6
C6 100pf



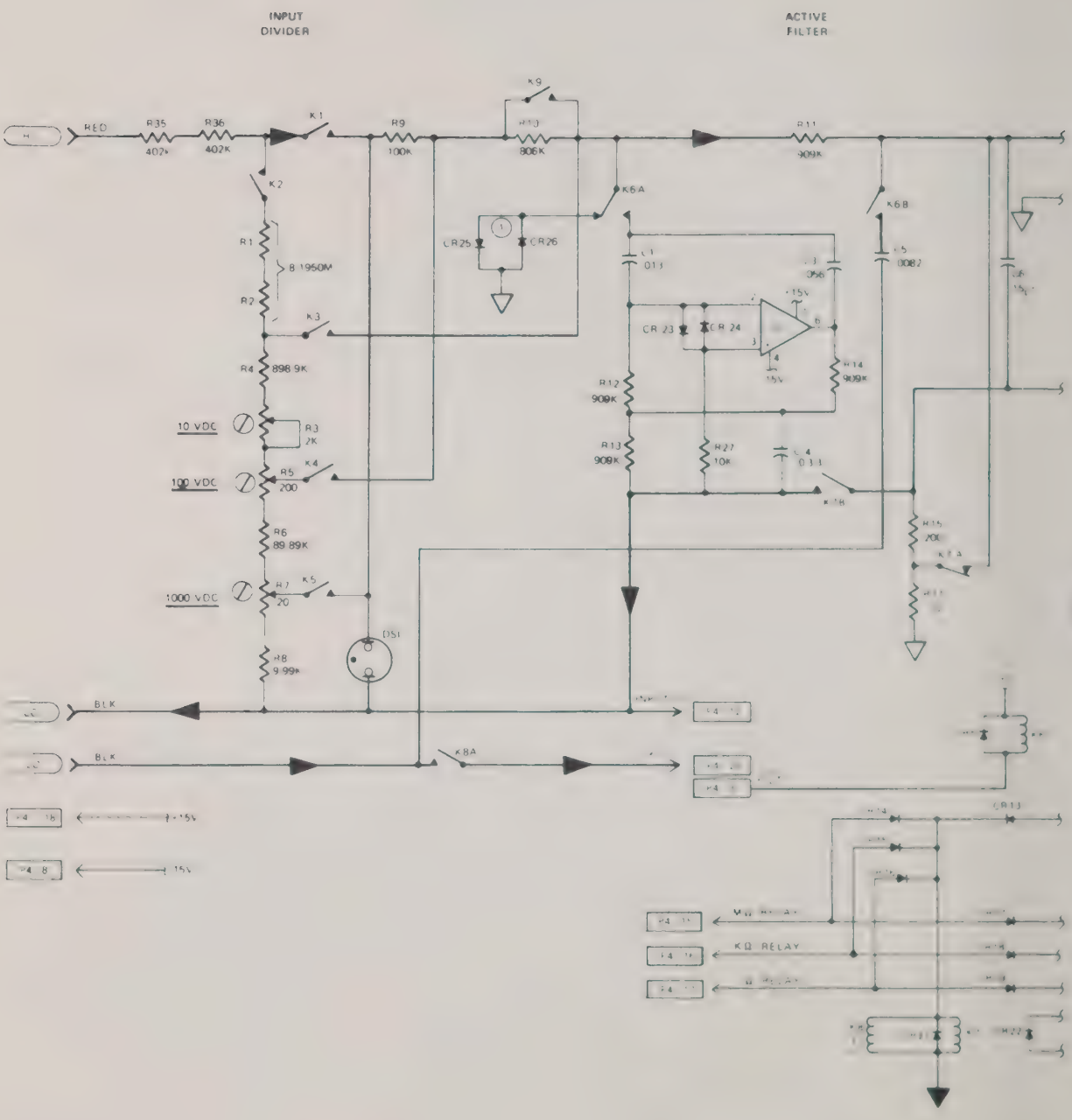
IC	PIN CONNECTIONS	
	+5V	COMMON
U1 U4	14	7

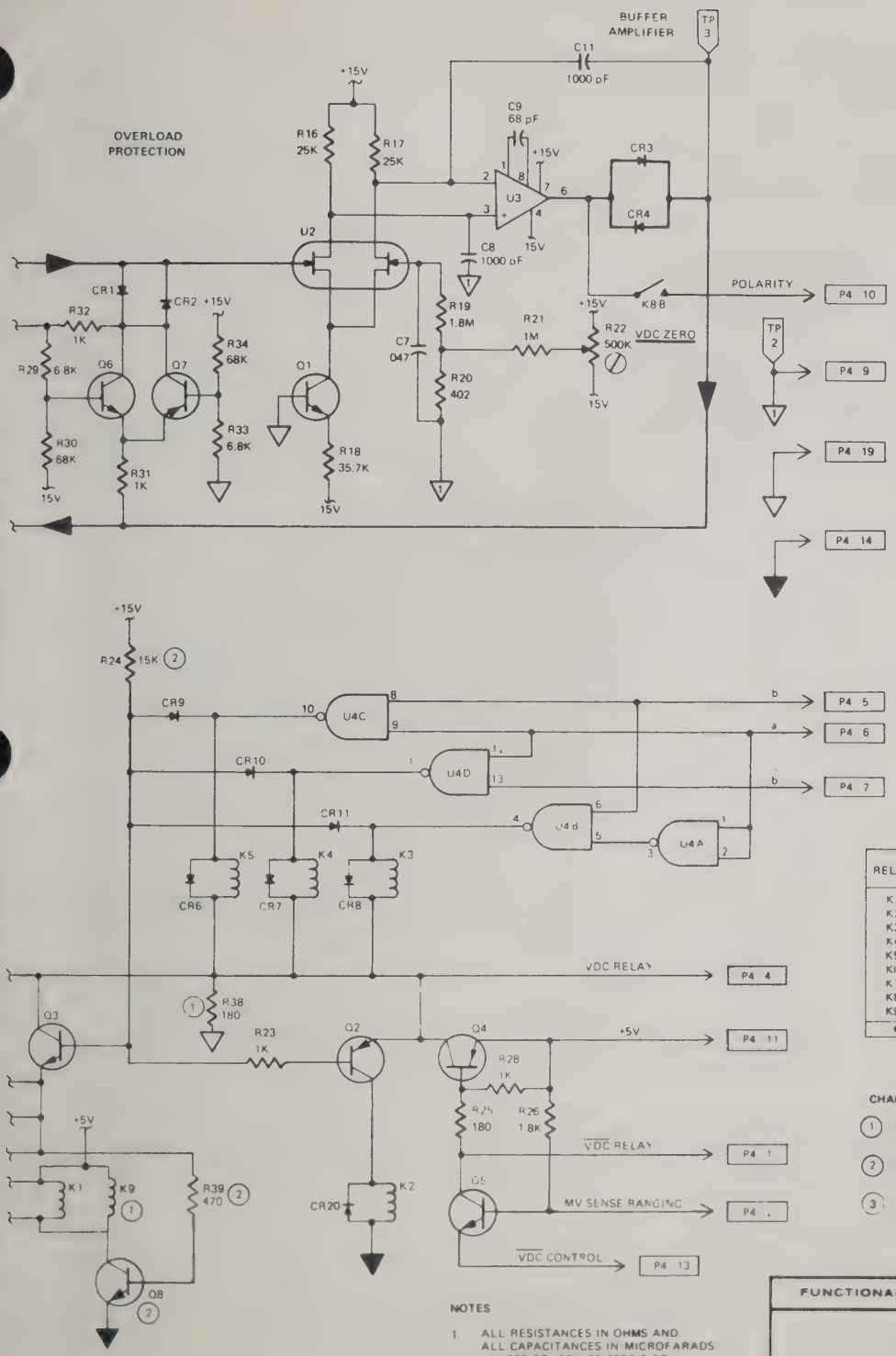
NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⊘ DENOTES INTERNAL ADJUSTMENT.
3. ▼ DENOTES LOGIC COMMON.
4. ▽ DENOTES BUFFER OUTPUT LOW.
5. ▭ DENOTES FRONT PANEL LOCATION
6. (1) FACTORY SELECTED RESISTORS.
7. ▬▶ DENOTES PRIMARY SIGNAL PATH.

CHANGES

(1) MOVED AND CHANGED VALUE OF C12 FROM 0.22 TO 2.2 IN SER. NO. 448 AND ON


INPUT
DIVIDER
ACTIVE
FILTER
K9
K1
K2
K3
K4
K5
K6A
K6B
K8A
R1
8.1950M
R2
R3
2K
R4
898.9K
R5
200
R6
89.89K
R7
20
R8
9.99K
R9
100K
R10
806K
R11
909K
R12
909K
R13
909K
R14
909K
R15
20K
R27
10K
C1
.013
C2
.056
C3
.0082
C4
.033
CR23
CR24
CR25
CR26
+15V
-15V
10 VDC
100 VDC
1000 VDC
DS1
BLK
BLK
K8 RELAY



IC	PIN CONNECTIONS	
	+5V	COMMON
U4	14	7

RELAY	VOLTAGE RANGE				FILTER
	1	10	100	1000	
K1	•				
K2		•	•	•	
K3		•			
K4			•		
K5				•	
K6					•
K7	•	•	•	•	
K8	•	•	•	•	
K9	•				

• DENOTES RELAY ENERGIZED

CHANGES

(1) R38, CR25, CR26, K8 and K9 added in Ser No. 329 and on

(2) R39, Q8 ADDED AND R24 CHANGED FROM 10K IN SER NO 580 AND ON

(3) C9 CHANGED FROM 68PF AND C8 CHANGED FROM 390PF AT SERIAL NO. 620 AND ON

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. DENOTES INTERNAL ADJUSTMENT
3. DENOTES BUFFER RETURN
4. DENOTES BUFFER OUTPUT LOW
5. DENOTES FRONT PANEL LOCATION
6. DENOTES LOGIC COMMON
7. DENOTES PRIMARY SIGNAL PATH

FUNCTIONAL SCHEMATIC DIAGRAM

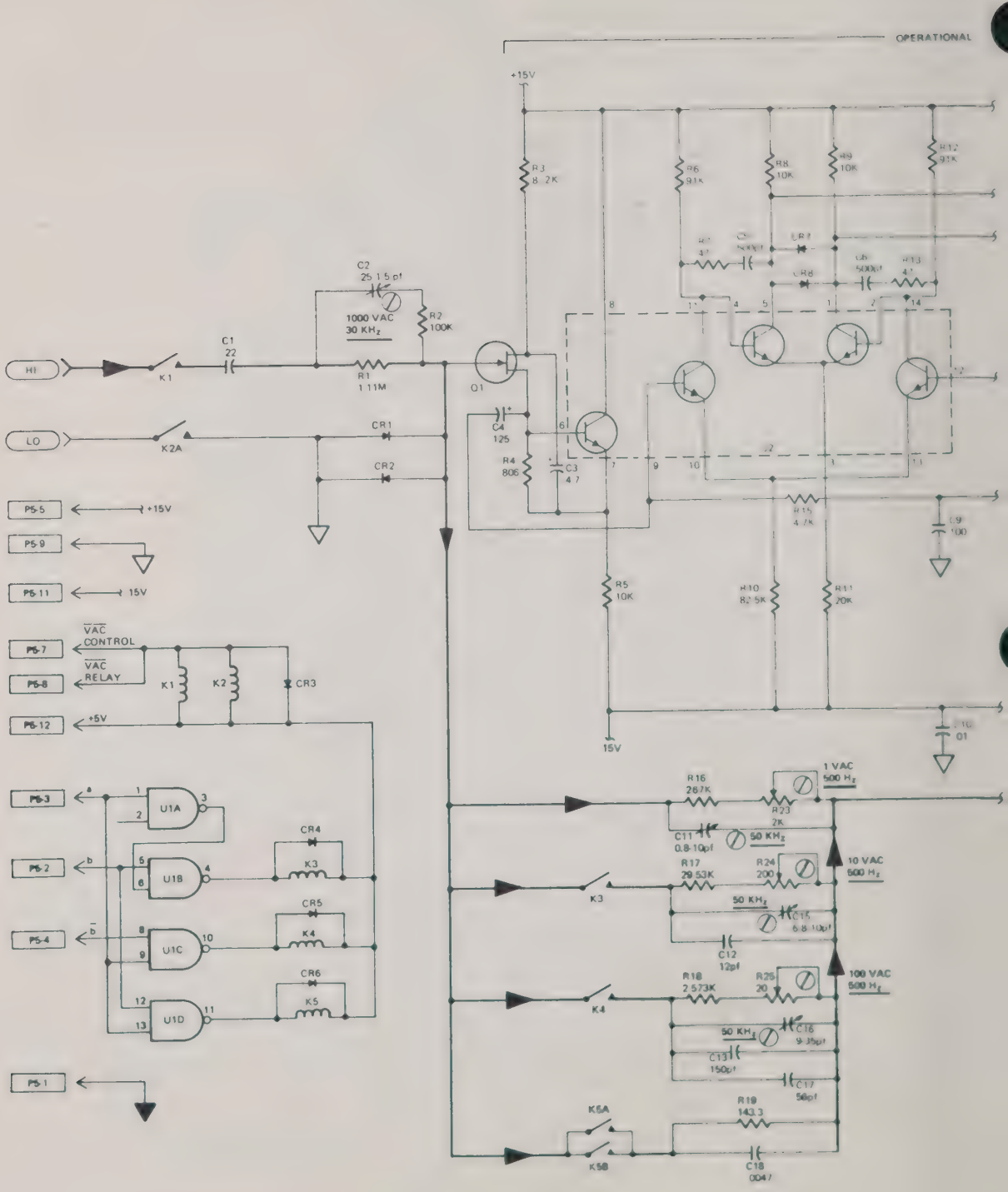
5

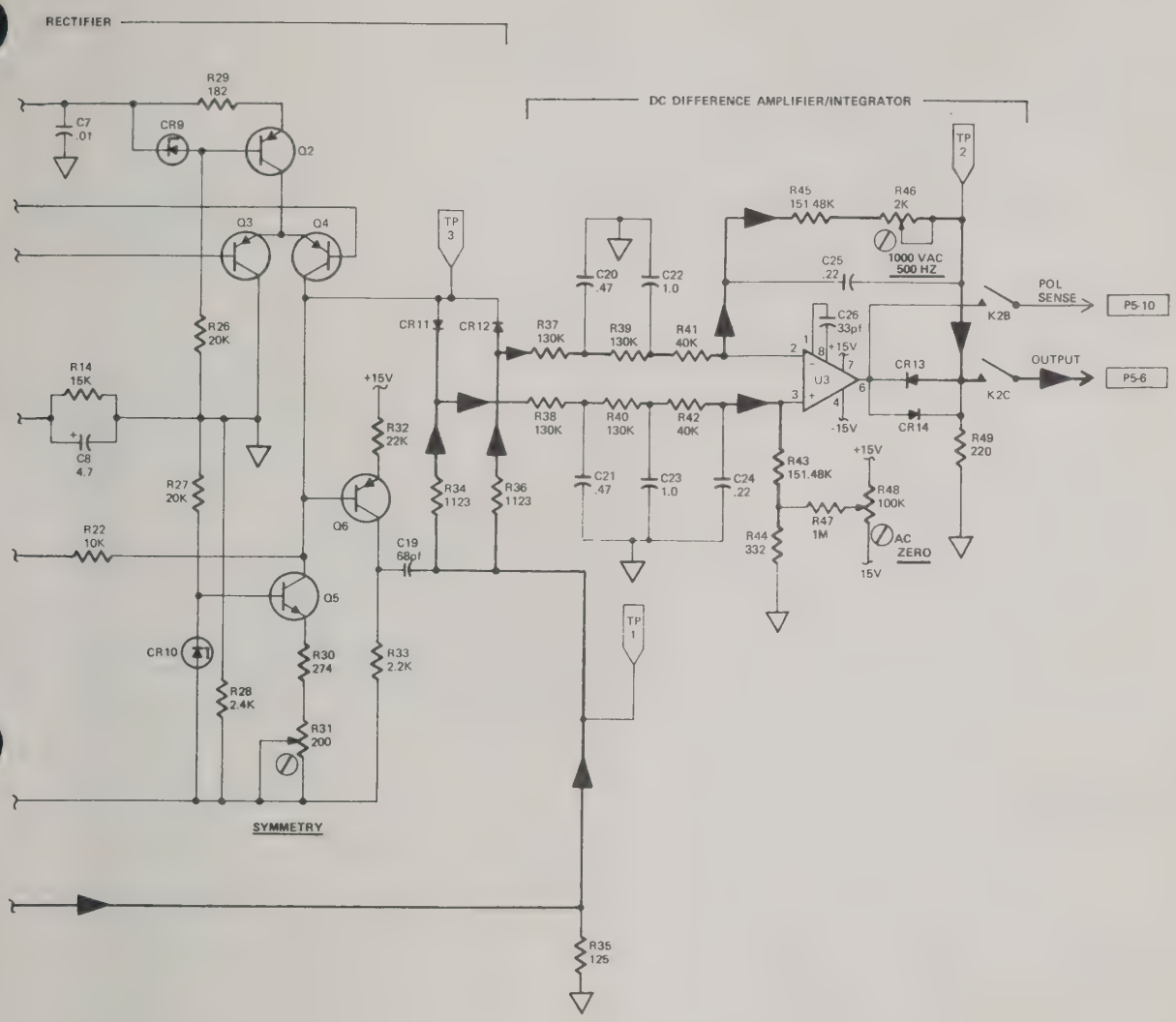
A4

INPUT BUFFER ASSEMBLY

Drawing No. 8200A-1004 Rev —

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


OPERATIONAL
+15V
R3 8.2K
R6 91K
R8 10K
R9 10K
R12 91K
C2 25 1.5 pf
1000 VAC 30 KHz
R2 100K
C1 22
HI
K1
R1 1.11M
LO
K2A
CR1
CR2
Q1
C4 125
R4 806
C3 4.7
P5-5 +15V
P5-9
P5-11 15V
P5-7 VAC CONTROL
P5-8 VAC RELAY
P5-12 +5V
K1
K2
CR3
R5 10K
R10 82.5K
R11 20K
R15 4.7K
C9 100
15V
C10 01
P5-3
P5-2
P5-4
P5-1
U1A
U1B
U1C
U1D
CR4
CR5
CR6
K3
K4
K5
R16 287K
R23 2K
1 VAC 500 Hz
C11 0.8-10pf
50 KHz
R17 29.53K
R24 200
10 VAC 500 Hz
C15 6.8-100pf
C12 12pf
R18 2.573K
R25 20
100 VAC 500 Hz
C16 9.35pf
C13 150pf
C17 56pf
R19 143.3
K5A
K5B
C18 0047



IC	PIN CONNECTIONS	
	+5V	COMMON
U1	14	7

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. ▼ DENOTES LOGIC COMMON
4. ▽ DENOTES SIGNAL COMMON
5. ▭ DENOTES FRONT PANEL LOCATION
6. ▬▶ DENOTES PRIMARY SIGNAL PATH.

FUNCTIONAL SCHEMATIC DIAGRAM	
6	
A5	
AC CONVERTER	
Drawing No. 8200A-1005	REV –

FLUKE JOHN FLUKE MFG. CO., INC
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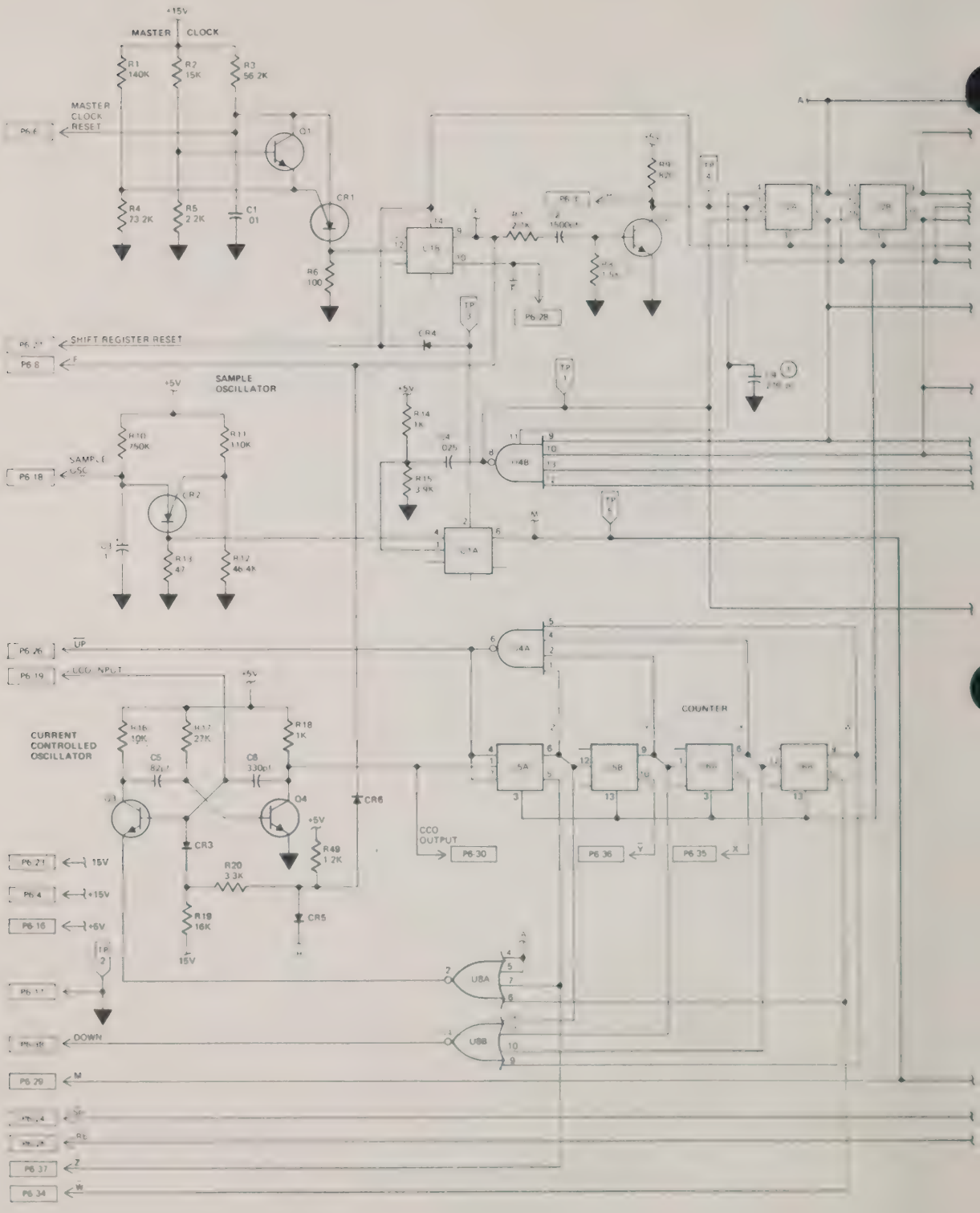
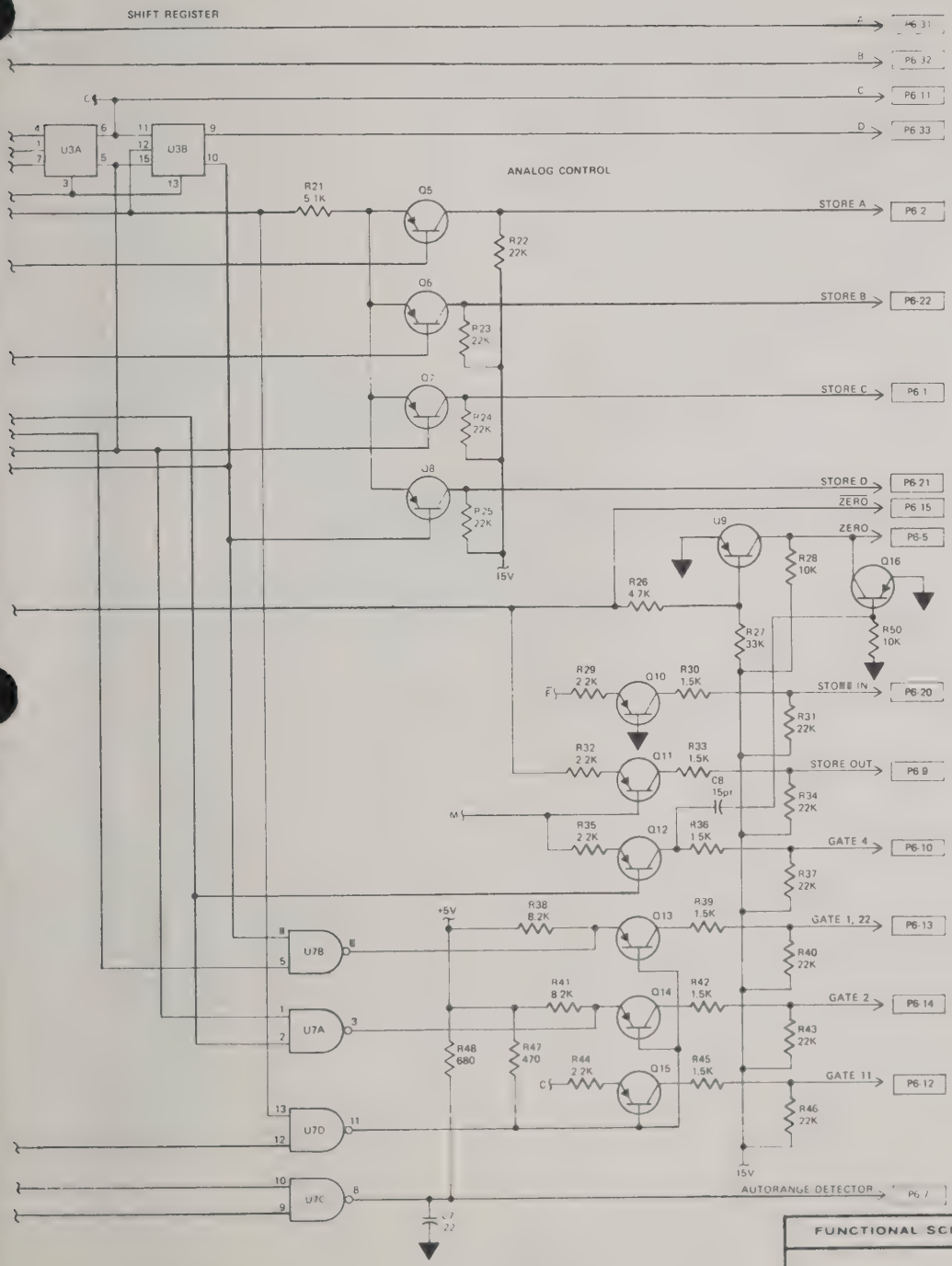

MASTER CLOCK
MASTER CLOCK RESET
SHIFT REGISTER RESET
SAMPLE OSCILLATOR
CURRENT CONTROLLED OSCILLATOR
COUNTER
CCO OUTPUT
UP
DOWN



NOTES

1 ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED

2 ▼ DENOTES LOGIC COMMON.

CHANGES

(1) C9 ADDED IN SER NO 438 AND ON

IC	PIN CONNECTIONS	
	+5V	COMMON
U7, U4	14	7
U1 U2, U3 U5 U6	16	8
U8	8	1

FUNCTIONAL SCHEMATIC DIAGRAM

7

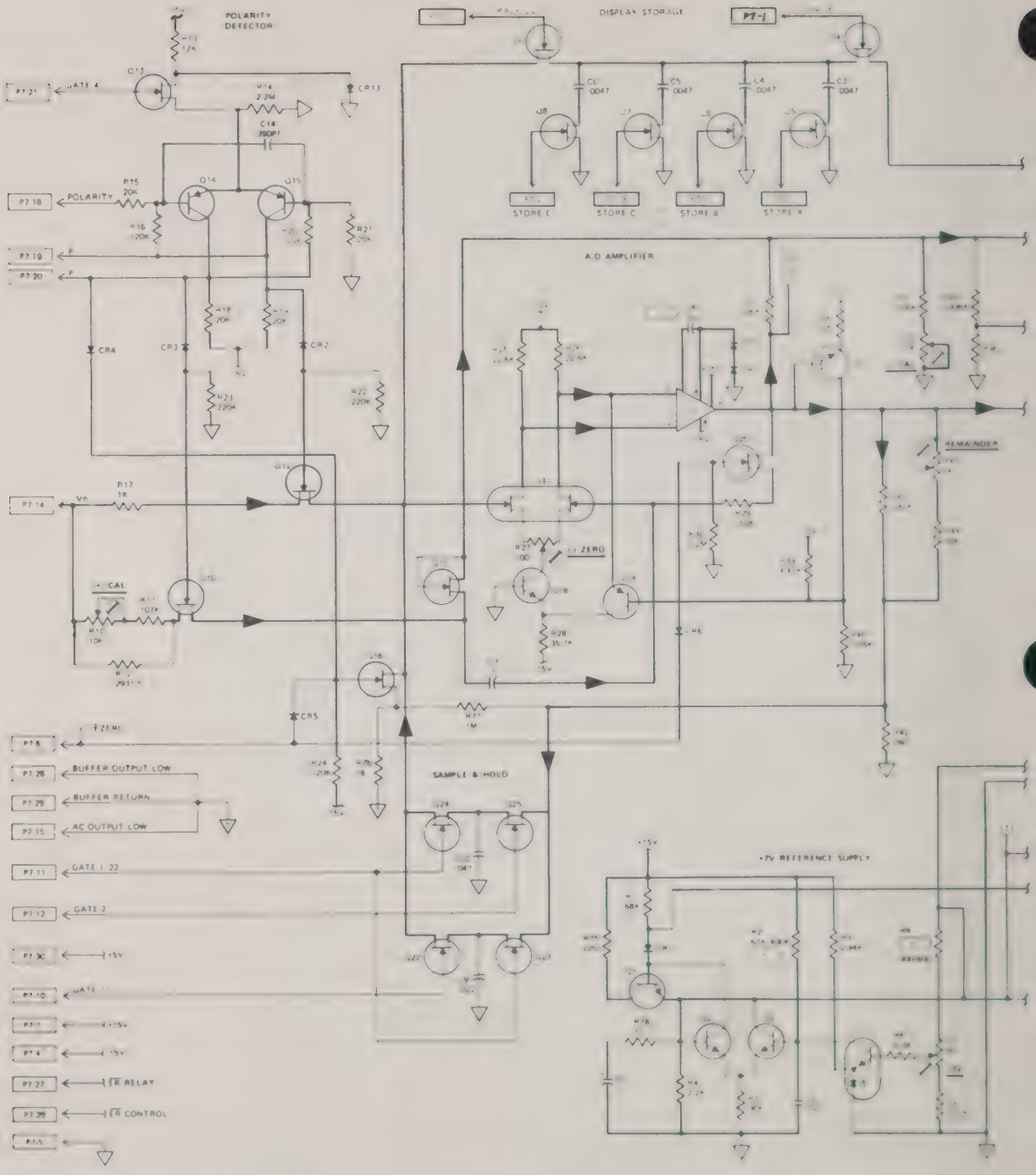
A6

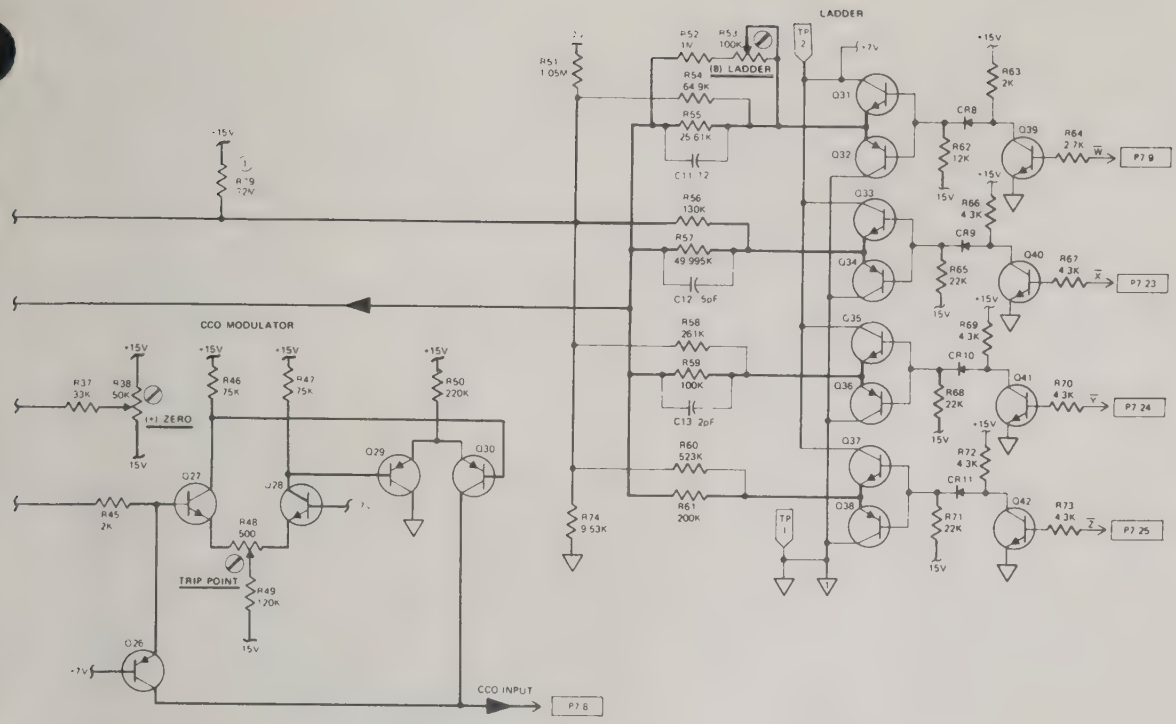
LOGIC CONTROL ASSEMBLY

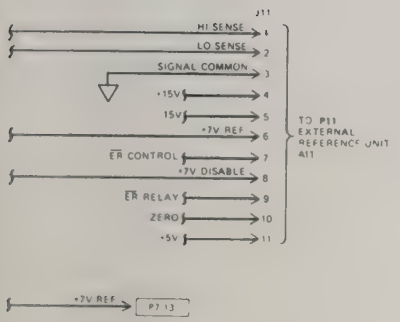
Drawing No. 8200A-1006

REV —

FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133


POLARITY DETECTOR
DISPLAY STORAGE
A-D AMPLIFIER
SAMPLE & HOLD
+7V REFERENCE SUPPLY
STORE D
STORE C
STORE B
STORE A
POLARITY
BUFFER OUTPUT LOW
BUFFER RETURN
AC OUTPUT LOW
GATE 1, 22
GATE 2
+5V
ER RELAY
ER CONTROL
CAL
ZERO
REMAINDER





CHANGES

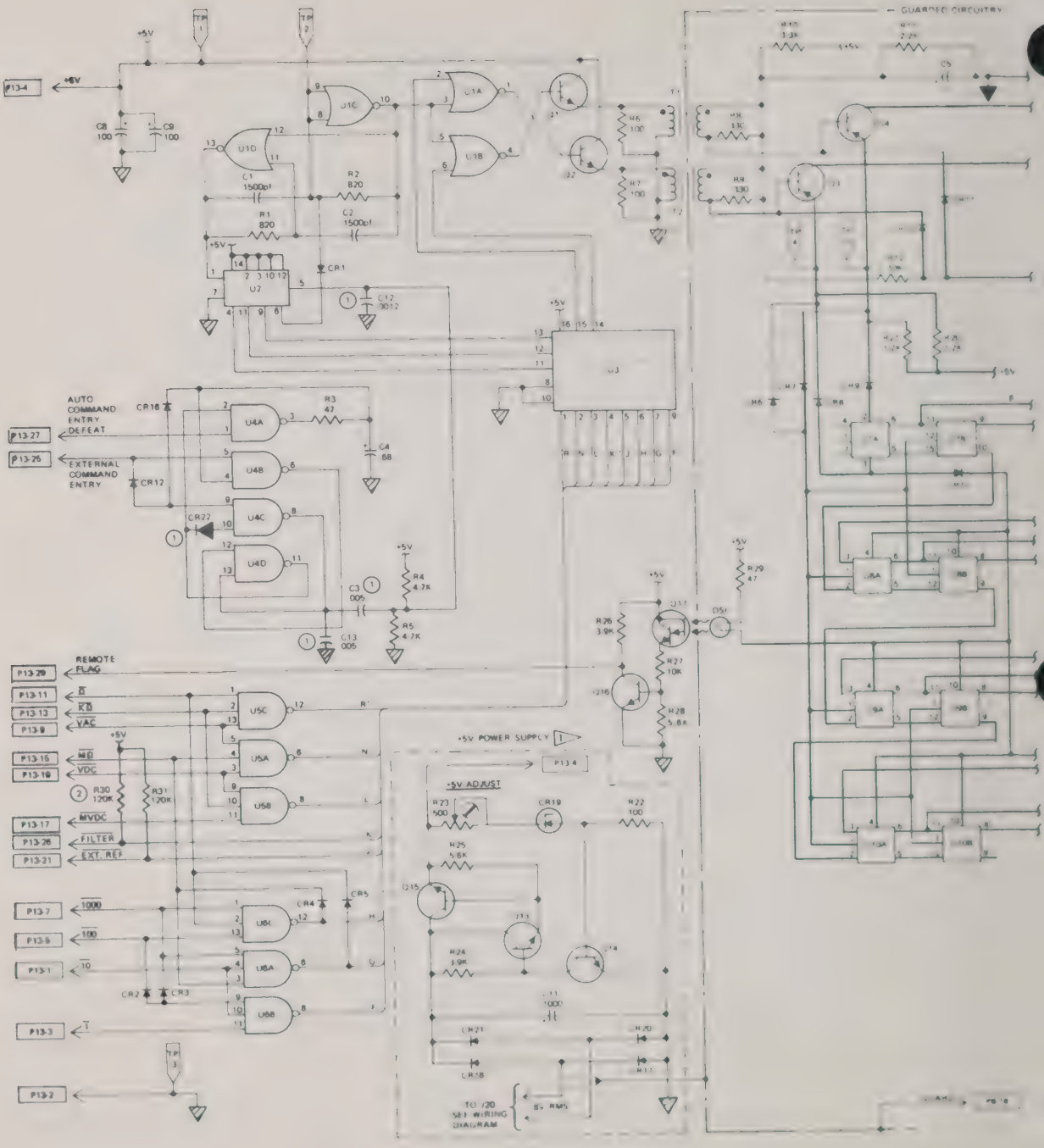
(1) R79 ADDED ON S N 34* AND ON

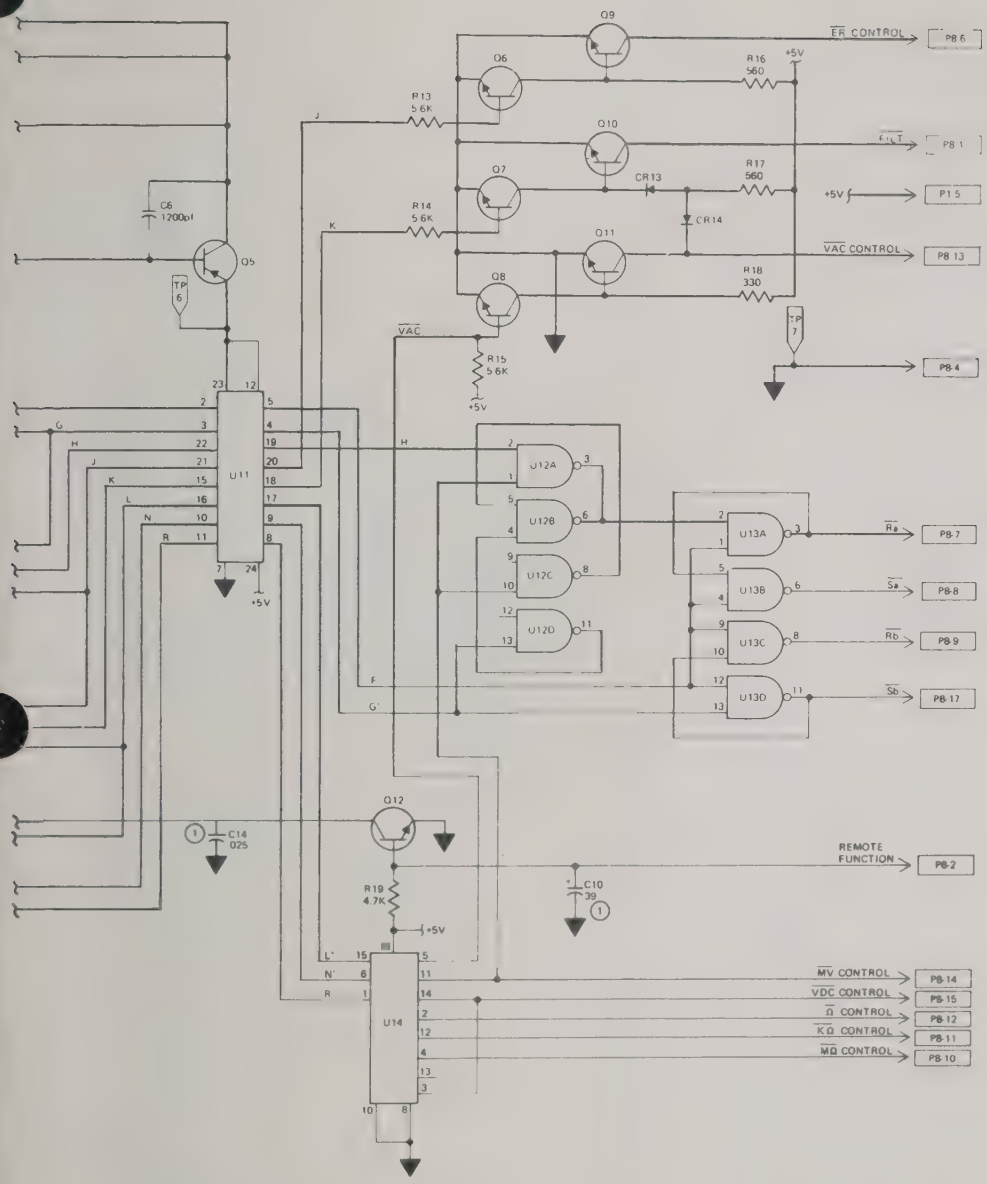
(2) ADD C14 AT SERIAL NO. 620 AND ON.

NOTES

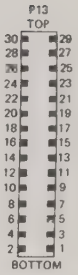
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT.
3. ▽ DENOTES SIGNAL COMMON
4. ▽ DENOTES A/D COMMON (CONNECTED TO SIGNAL COMMON AT TP1)
5. 1 DENOTES FACTORY SELECTED COMPONENT (NOMINAL VALUE SHOWN).
6. ▬▶ DENOTES PRIMARY SIGNAL PATH

FUNCTIONAL SCHEMATIC DIAGRAM	
8	
A7	
A/D ANALOG ASSEMBLY	
Drawing No. 8200A-1007	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


GUARDED CIRCUITRY
AUTO COMMAND ENTRY DEFEAT
EXTERNAL COMMAND ENTRY
REMOTE FLAG
+5V POWER SUPPLY
-5V ADJUST
TO J20 SEE WIRING DIAGRAM



P13 PIN CONNECTIONS AS VIEWED FROM REAR OF INSTRUMENT



IC	PIN CONNECTIONS	
	+5V	COMMON
U1, U4 U6, U8 10, U12 U13	14	7
U3, U7	16	8

CHANGES:

(1) ADDED C12, C13, C14, CR22 AND CHANGED C3 AND C10 IN SER. NO 183 AND ON.

(2) ADDED R30, R31 IN SER. NO. 148 AND ON

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. DENOTES INTERNAL ADJUSTMENT.
3. DENOTES LOGIC COMMON.
4. DENOTES EXTERNAL GROUND OR COMMON.
5. (1) THIS POWER SUPPLY INSTALLED ONLY IN SPECIAL RCU, 8200A-08/AA. PROVIDES +5V LOGIC POWER TO RCU EXTERNAL GUARD CIRCUITRY IN LIEU OF DOU OR POU LOGIC SUPPLIES WHEN THESE OPTIONS ARE NOT INSTALLED CONTACT FACTORY FOR DETAILS

FUNCTIONAL SCHEMATIC DIAGRAM

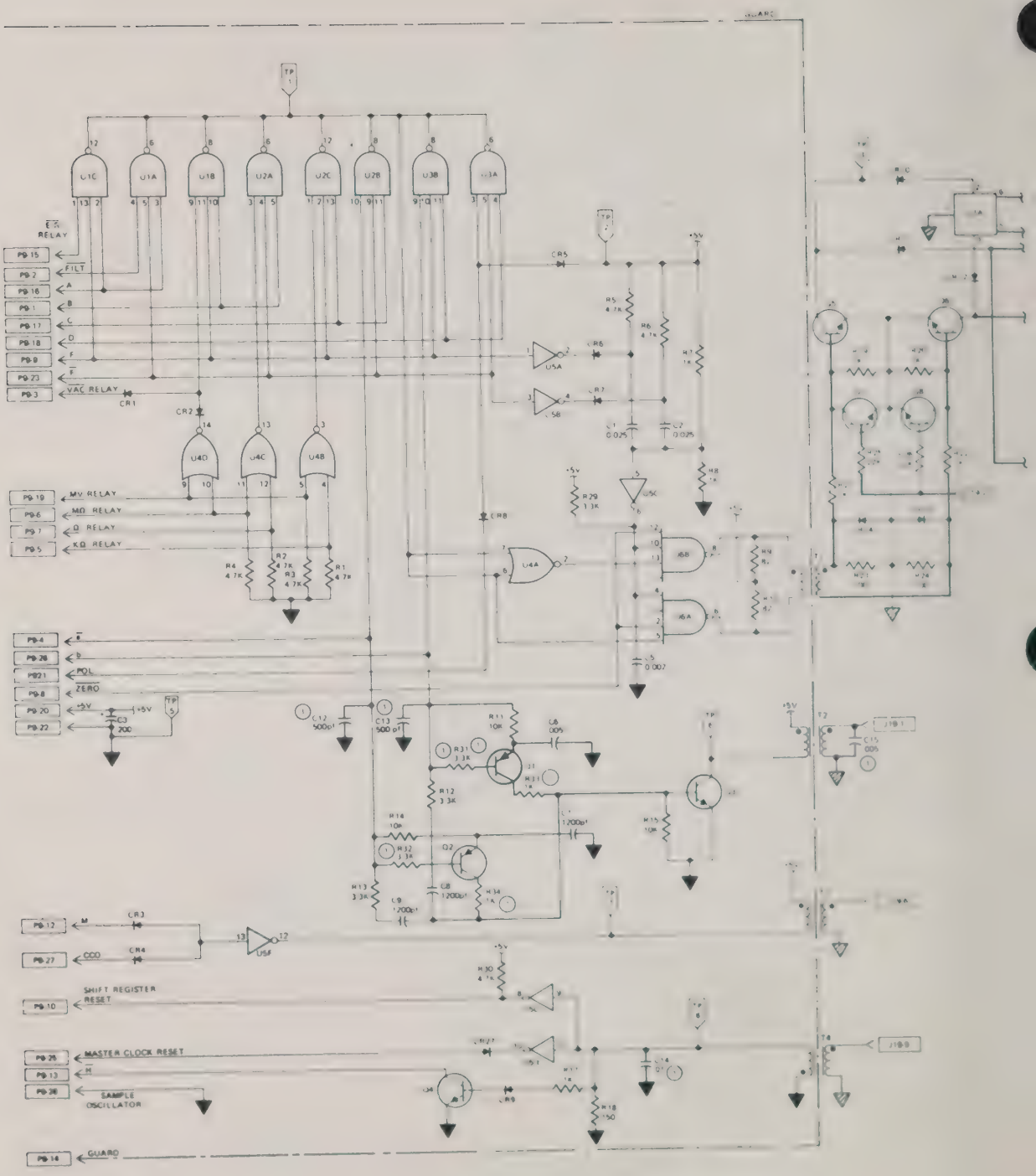
9

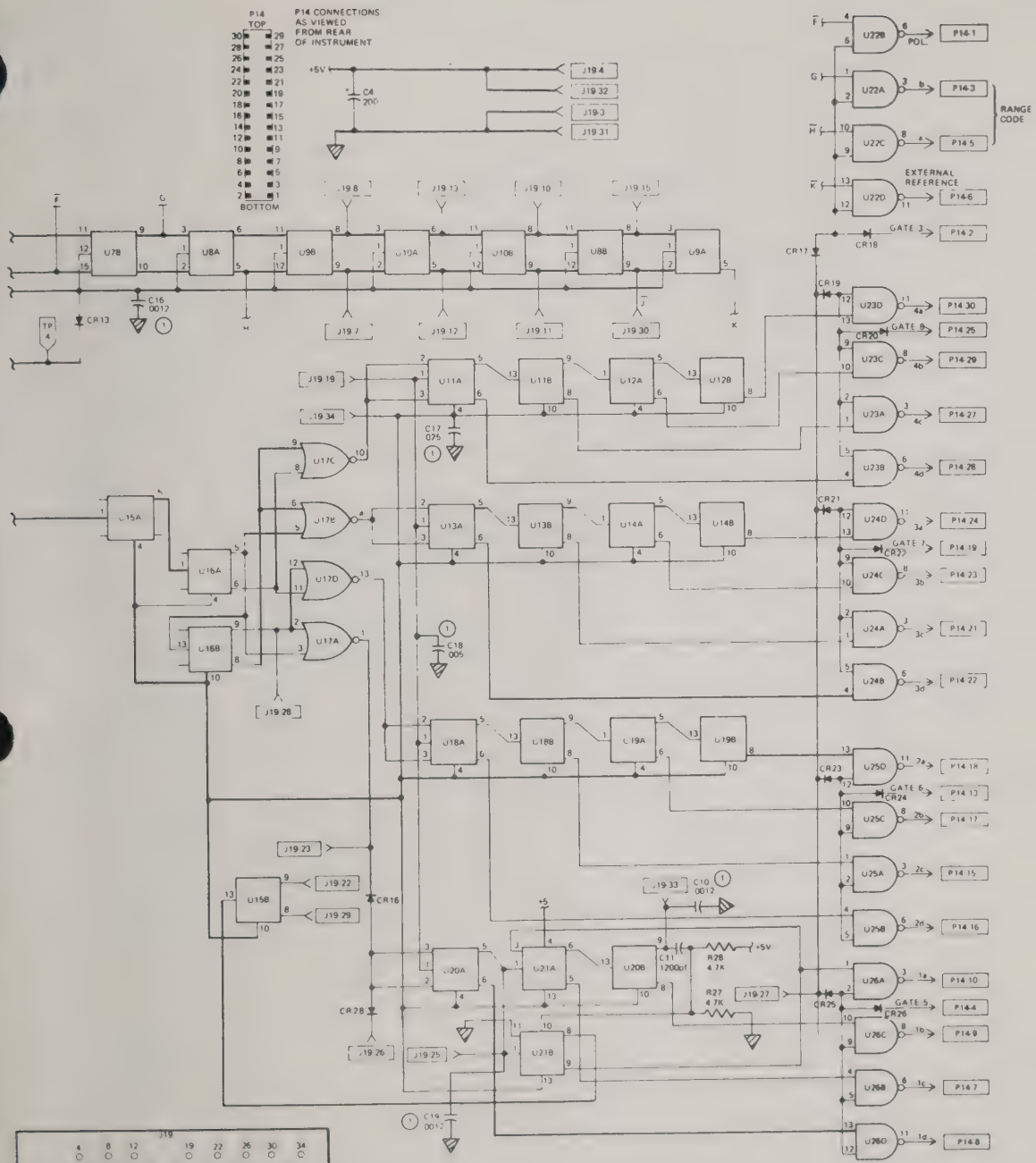
A8

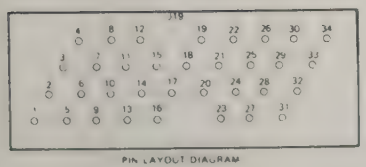
REMOTE CONTROL ASSEMBLY

Drawing No. 8200A-1008 Rev —

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle Washington 98133


U1C
U1A
U1B
U2A
U2C
U2B
U3B
U3A
RELAY
FILT
A
B
C
D
E
VAC RELAY
MV RELAY
MΩ RELAY
Ω RELAY
KΩ RELAY
ZERO
+5V
MASTER CLOCK RESET
SAMPLE OSCILLATOR
SHIFT REGISTER RESET
GUARD





PIN LAYOUT DIAGRAM

IC	PIN CONNECTION	
	+5V	COMMON
U1 3 5 6 U8 26	14	7
U4	8	1
U7	16	8

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACTANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. DENOTES EXTERNAL GROUND OR COMMON
3. DENOTES LOGIC COMMON
4. HARD WIRED CONNECTOR CABLE MATES WITH J19 ON THIS ASSEMBLY AND CONNECTS TO J19 ON DOU ASSEMBLY NO. 2 (A10)

CHANGES

(1) ADDED C10, C12 THROUGH C19, R31 THROUGH R34. CHANGED C6 AND C7 IN SER. NO. 188 AND ON

FUNCTIONAL SCHEMATIC DIAGRAM

10

A9

DATA OUTPUT UNIT–1

Drawing No. 8200A-1009

Rev

–

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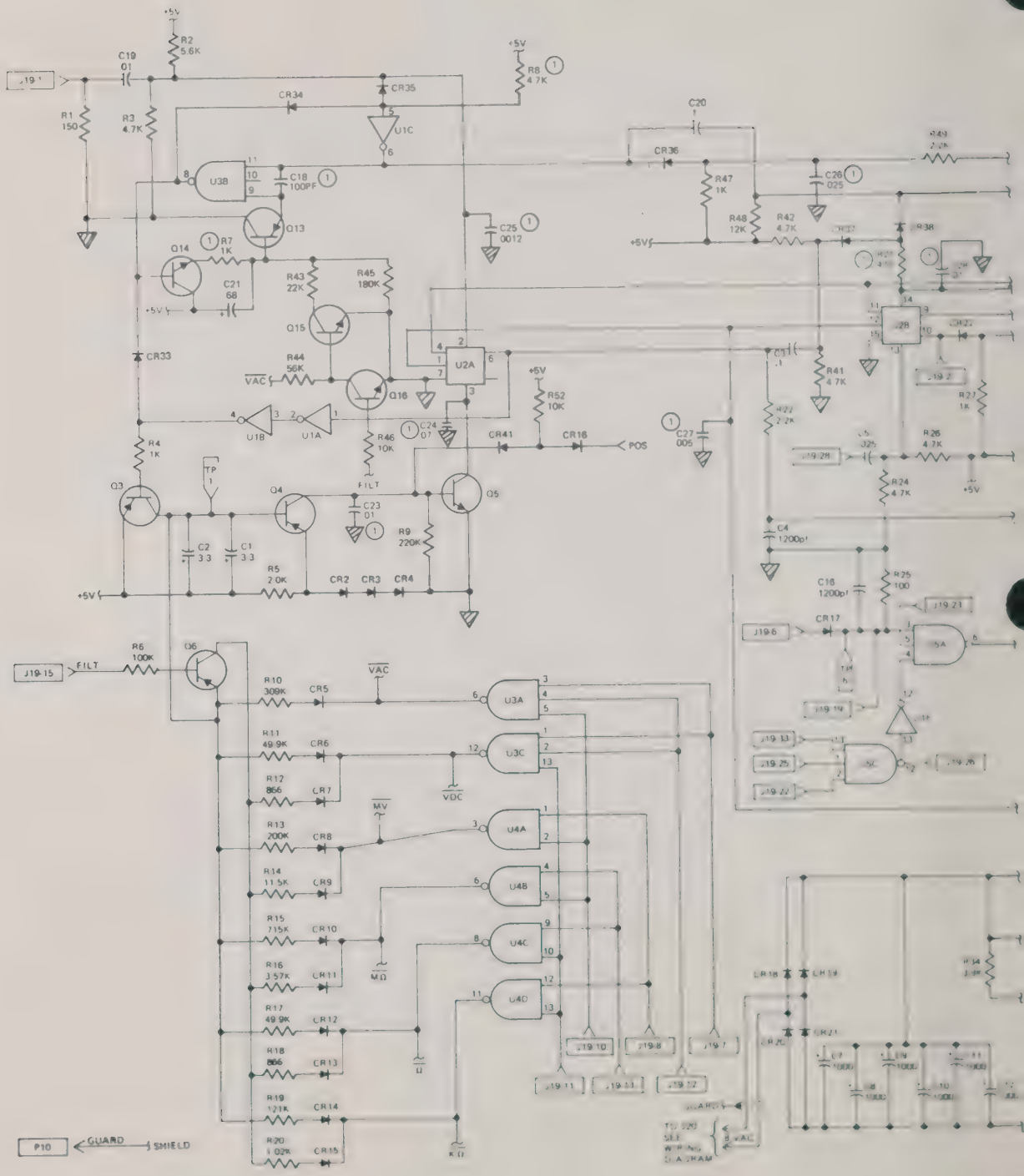
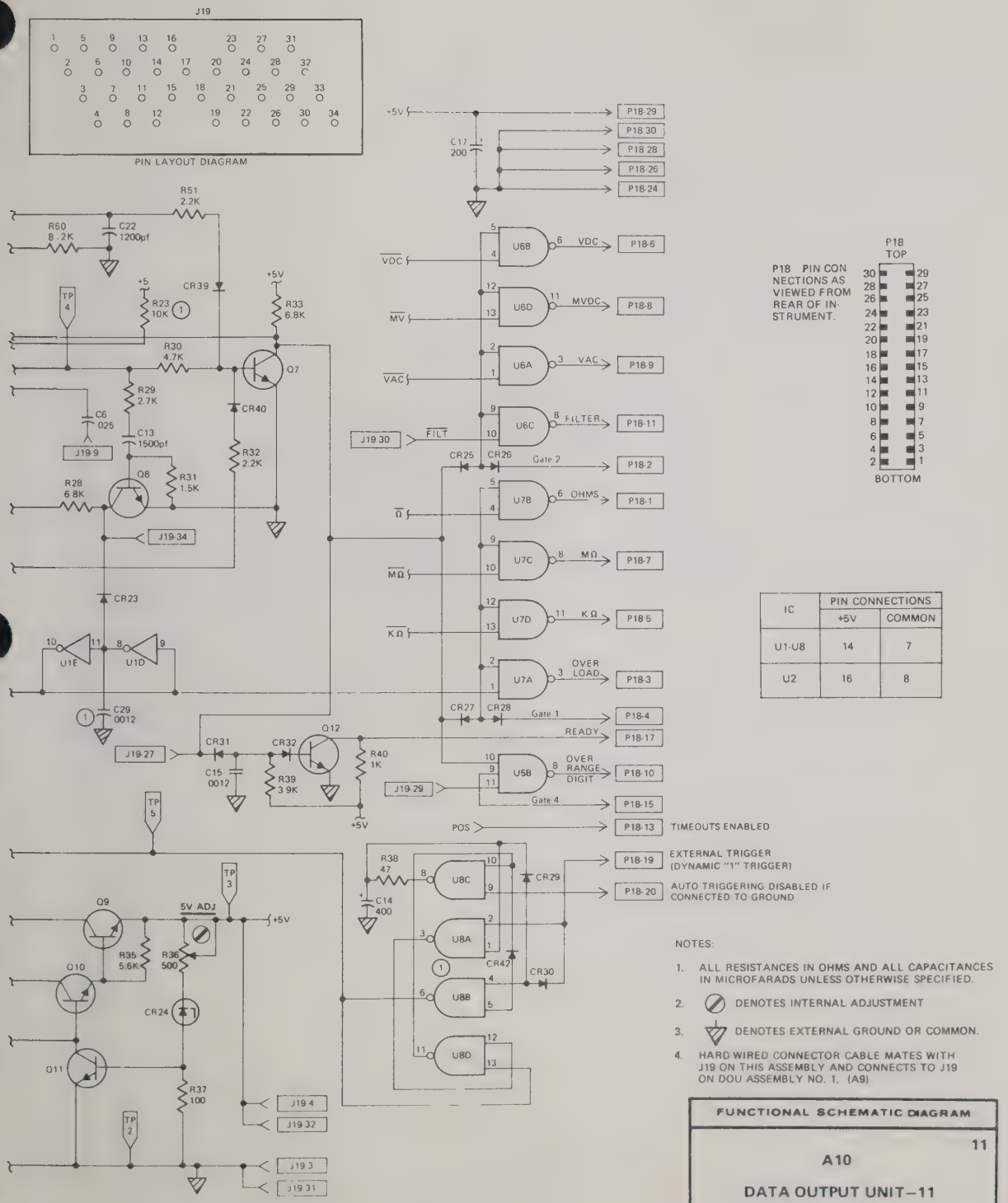

+5V
R2 5.6K
C19 01
J19-1
R1 150
R3 4.7K
CR34
CR35
U1C
R8 4.7K
U3B
C18 100PF
Q13
Q14
R7 1K
C21 68
R43 22K
R45 180K
Q15
C25 0012
CR33
R44 56K
VAC
Q16
U2A
R52 10K
U1B
U1A
C24 07
CR41
CR16
POS
R4 1K
Q3
TP 1
Q4
FILT
C23 01
Q5
C2 3.3
C1 3.3
R9 220K
R5 2.0K
CR2
CR3
CR4
C20
CR36
R47 1K
C26 025
R48 12K
R42 4.7K
R41 4.7K
R27 1K
R26 4.7K
R24 4.7K
C4 1200pf
C16 1200pf
R25 100
CR17
J19-6
J19-15
R6 100K
Q6
R10 309K
CR5
R11 49.9K
CR6
R12 866
CR7
R13 200K
CR8
R14 11.5K
CR9
R15 715K
CR10
R16 3.57K
CR11
R17 49.9K
CR12
R18 866
CR13
R19 121K
CR14
R20 1.02K
CR15
MV
VDC
MΩ
KΩ
U3A
U3C
U4A
U4B
U4C
U4D
J19-10
J19-8
J19-7
J19-11
J19-12
P10
GUARD
SHIELD



P18 PIN CONNECTIONS AS VIEWED FROM REAR OF INSTRUMENT.

IC	PIN CONNECTIONS	
	+5V	COMMON
U1-U8	14	7
U2	16	8

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. ⏚ DENOTES EXTERNAL GROUND OR COMMON.
4. HARD WIRED CONNECTOR CABLE MATES WITH J19 ON THIS ASSEMBLY AND CONNECTS TO J19 ON DOU ASSEMBLY NO. 1. (A9)

CHANGES:

(1) ADDED C23 THROUGH C29, R7, R8, R21, R23 AND CR42 IN SER NO 188 AND ON.

(2) DELETED CR42 AT SERIAL NO. 180 AND ON.

FUNCTIONAL SCHEMATIC DIAGRAM

11

A10

DATA OUTPUT UNIT–11

Drawing No. 8200A-1010

REV —

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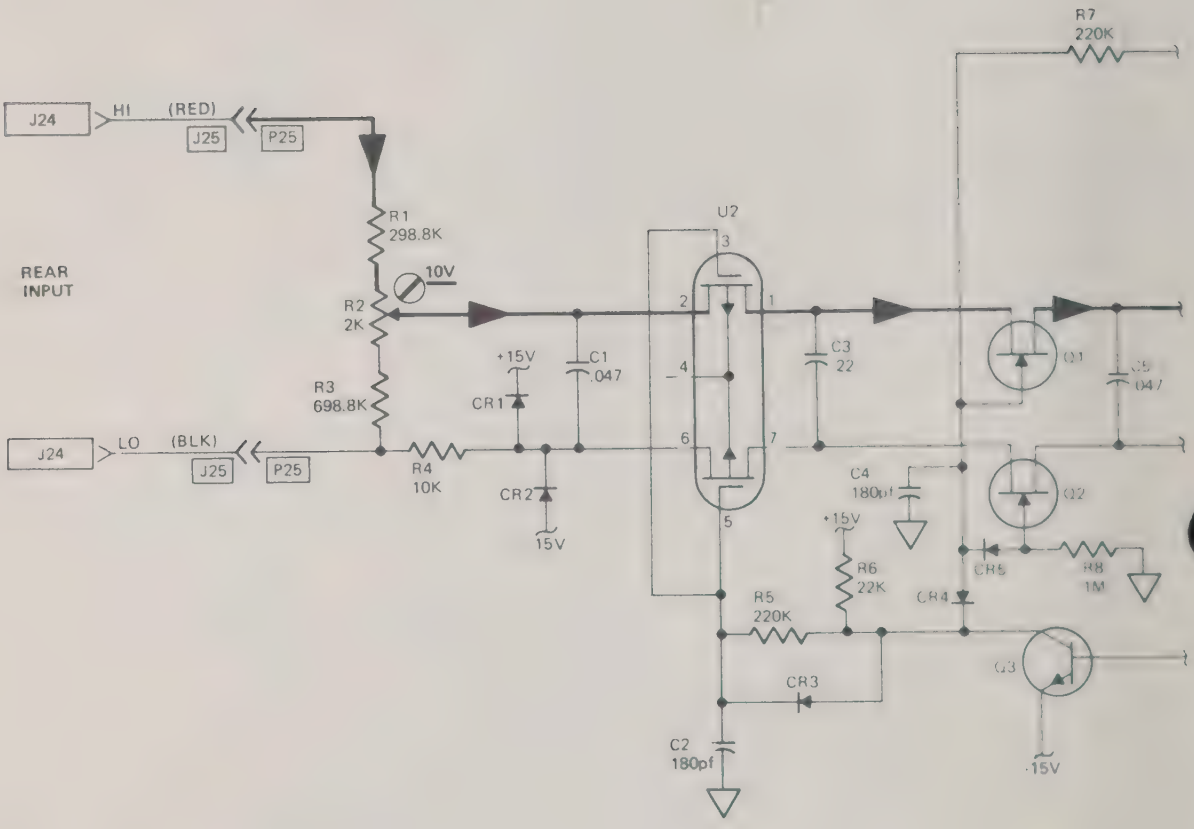
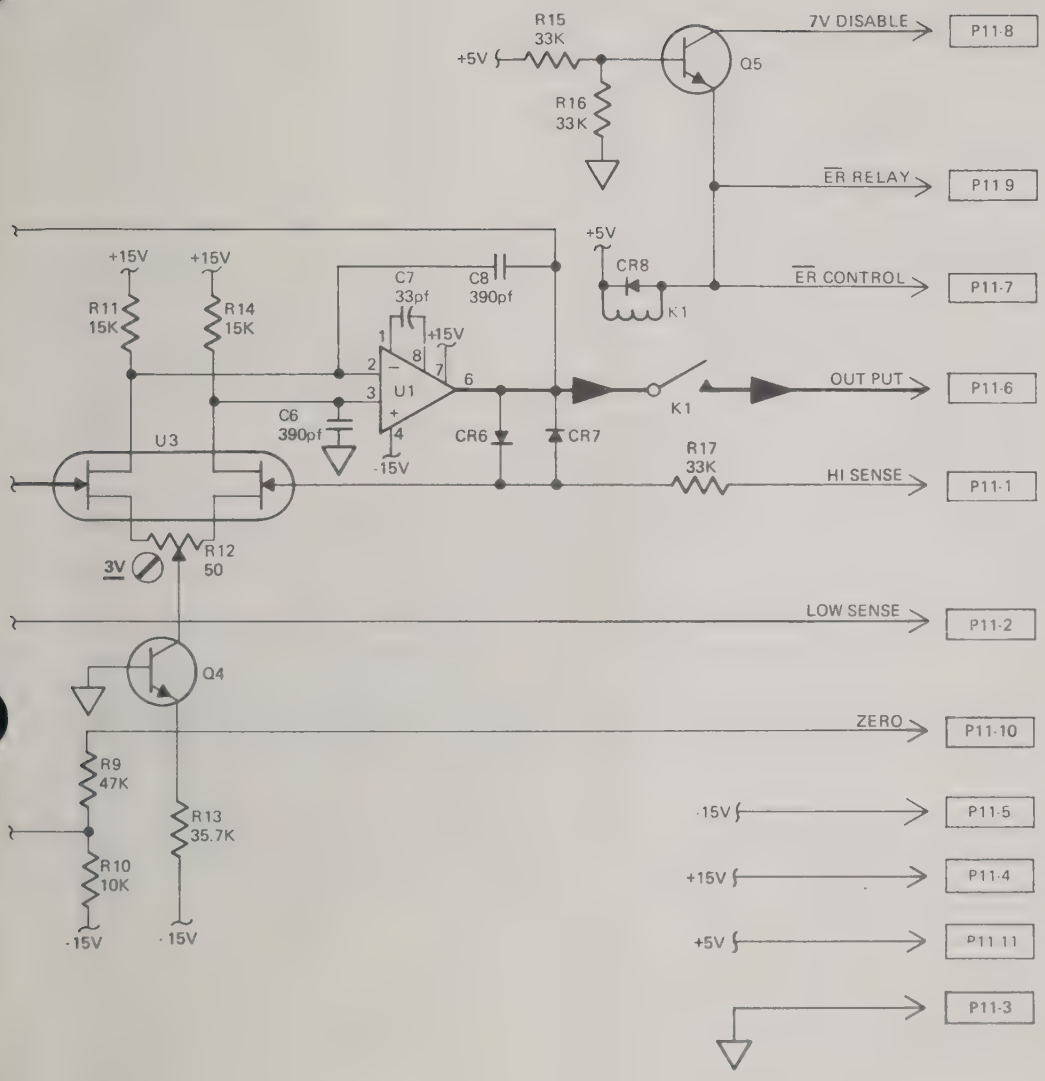
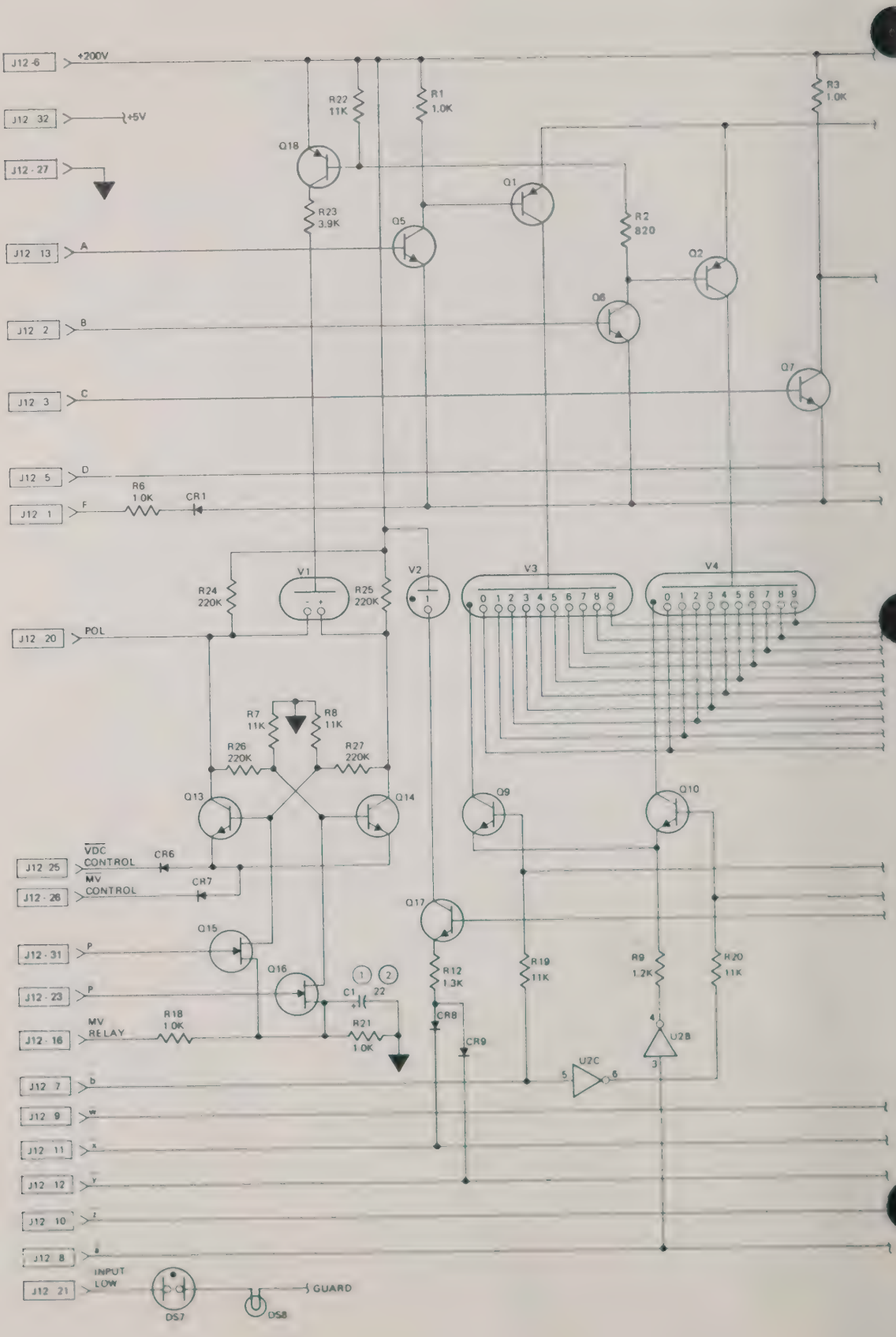

J24
HI
(RED)
J25
P25
R1
298.8K
REAR
INPUT
10V
R2
2K
R3
698.8K
J24
LO
(BLK)
J25
P25
R4
10K
+15V
CR1
C1
.047
CR2
15V
U2
3
2
1
4
6
7
5
C3
22
R7
220K
Q1
C5
.047
C4
180pf
Q2
+15V
R6
22K
CR5
R8
1M
CR4
R5
220K
Q3
CR3
C2
180pf
-15V

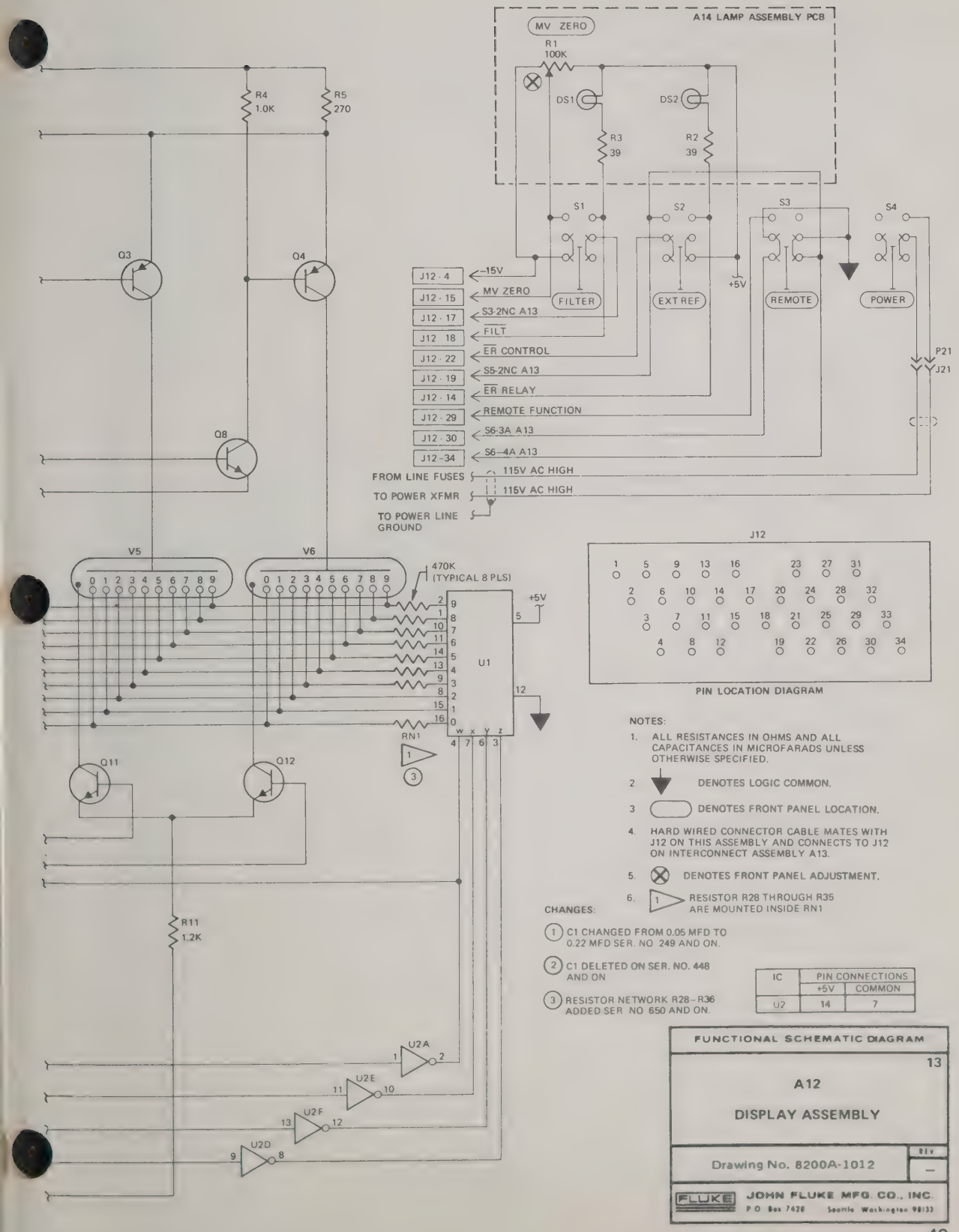


NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT.
3. ▽ DENOTES SIGNAL COMMON
4. → DENOTES PRIMARY SIGNAL PATH

FUNCTIONAL SCHEMATIC DIAGRAM	
12	
A11	
EXTERNAL REFERENCE ASSEMBLY	
Drawing No. 8200A-1011	REV –
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


J12-6
+200V
J12 32
+5V
J12 27
J12 13
A
J12 2
B
J12 3
C
J12 5
D
J12 1
F
R6
1.0K
CR1
R22
11K
R1
1.0K
R3
1.0K
Q18
R23
3.9K
Q5
Q1
R2
820
Q2
Q6
Q7
V1
V2
V3
V4
R24
220K
R25
220K
J12 20
POL
R7
11K
R8
11K
R26
220K
R27
220K
Q13
Q14
Q9
Q10
J12 25
VDC
CONTROL
CR6
J12 26
MV
CONTROL
CR7
Q17
Q15
J12 31
P
J12 23
P
Q16
C1
22
R12
1.3K
R19
11K
R9
1.2K
R20
11K
J12 16
MV
RELAY
R18
1.0K
R21
1.0K
CR8
CR9
U2B
U2C
J12 7
b
J12 9
w
J12 11
x
J12 12
y
J12 10
z
J12 8
a
J12 21
INPUT
LOW
DS7
DS8
GUARD



J12

PIN LOCATION DIAGRAM

NOTES:

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON.
3. ⬭ DENOTES FRONT PANEL LOCATION.
4. HARD WIRED CONNECTOR CABLE MATES WITH J12 ON THIS ASSEMBLY AND CONNECTS TO J12 ON INTERCONNECT ASSEMBLY A13.
5. ⊗ DENOTES FRONT PANEL ADJUSTMENT.
6. 1 RESISTOR R28 THROUGH R35 ARE MOUNTED INSIDE RN1

CHANGES:

(1) C1 CHANGED FROM 0.05 MFD TO 0.22 MFD SER. NO 249 AND ON.

(2) C1 DELETED ON SER. NO. 448 AND ON

(3) RESISTOR NETWORK R28–R36 ADDED SER NO 650 AND ON.

IC	PIN CONNECTIONS	
	+5V	COMMON
U2	14	7

FUNCTIONAL SCHEMATIC DIAGRAM

13

A12

DISPLAY ASSEMBLY

Drawing No. 8200A-1012

REV —

FLUKE JOHN FLUKE MFG. CO., INC.
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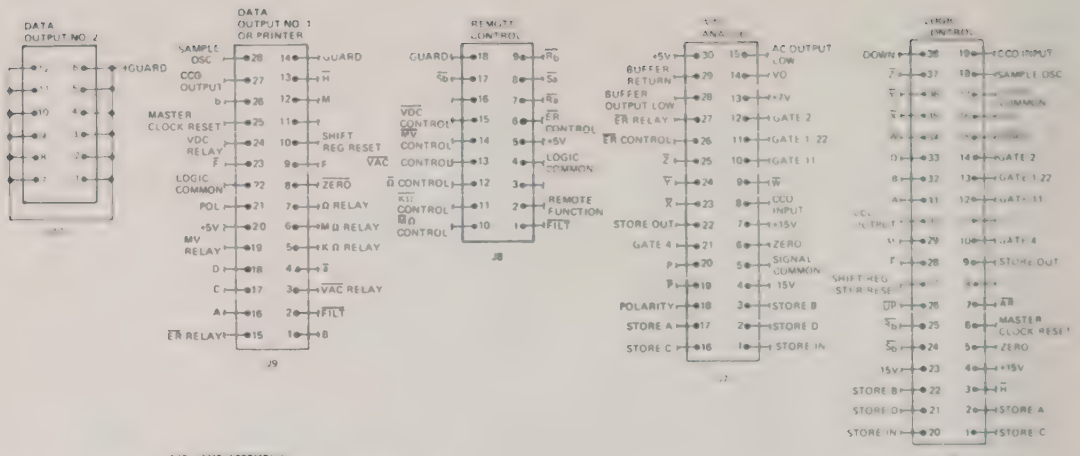
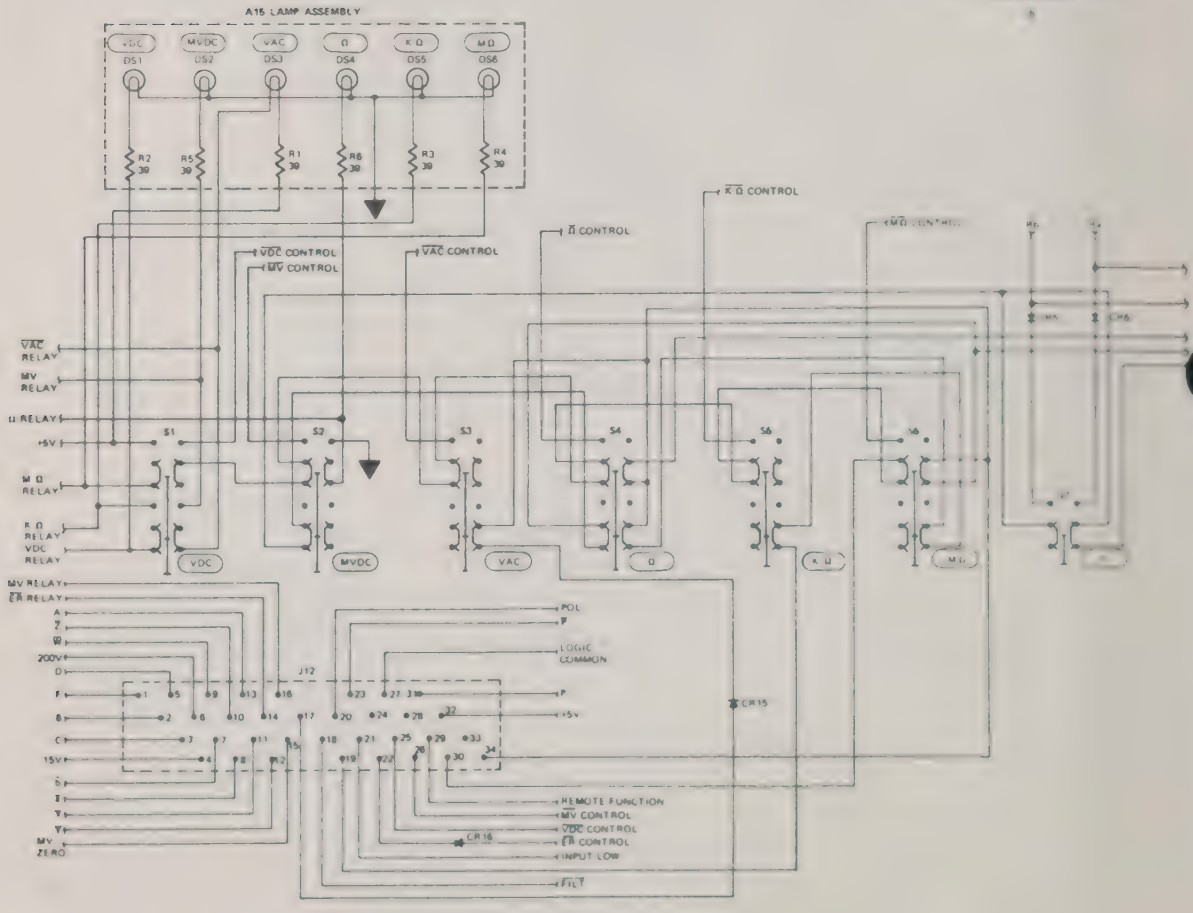
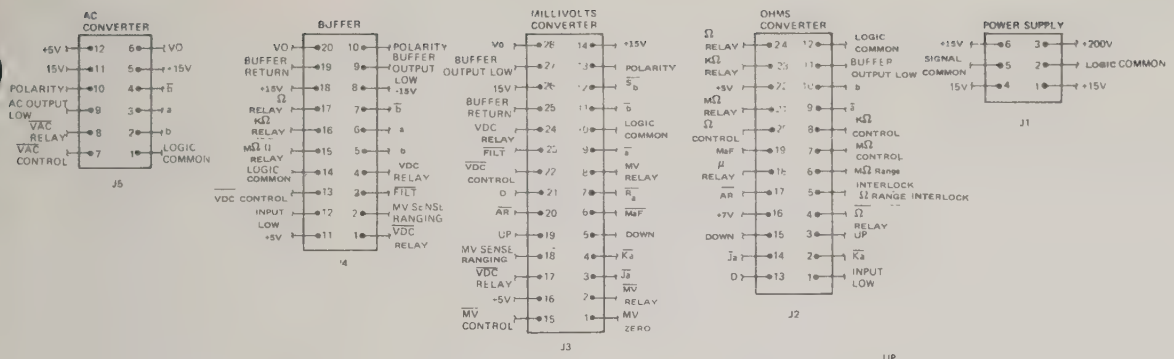
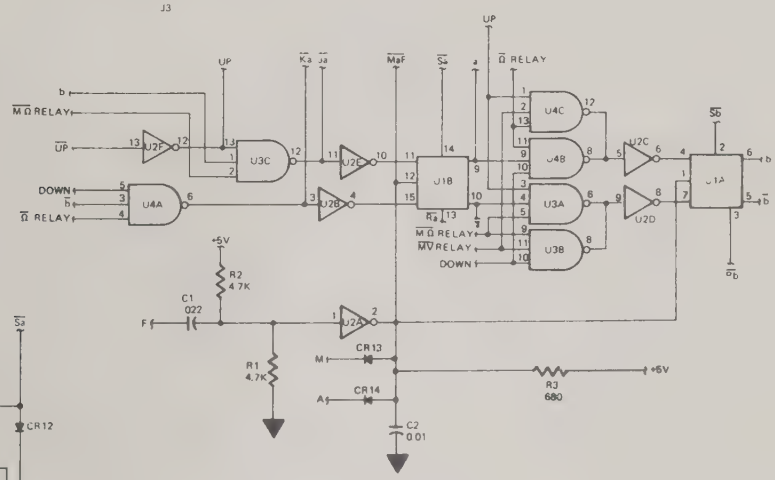
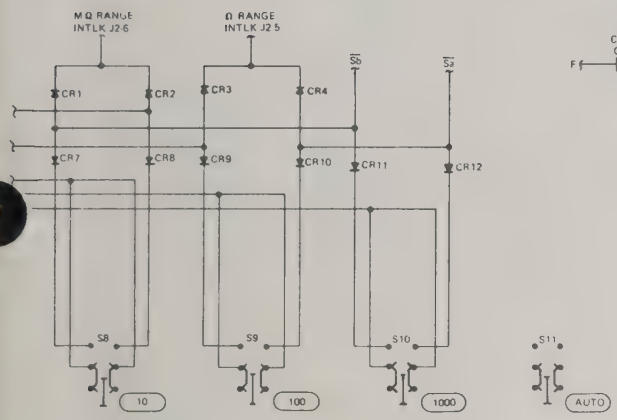

DATA OUTPUT NO. 2
DATA OUTPUT NO. 1 OR PRINTER
SAMPLE OSC
CCD OUTPUT
MASTER CLOCK RESET
VDC RELAY
LOGIC COMMON
POL
+5V
MV RELAY
ER RELAY
GUARD
SHIFT REG RESET
ZERO
Ω RELAY
MΩ RELAY
KΩ RELAY
VAC RELAY
FILT
J9
REMOTE CONTROL
REMOTE FUNCTION
J8
AC OUTPUT LOW
BUFFER RETURN
BUFFER OUTPUT LOW
GATE 2
GATE 1
STORE OUT
SIGNAL COMMON
STORE B
STORE D
STORE IN
STORE A
STORE C
J2
LOGIC CONTROL
CCD INPUT
SAMPLE OSC
GATE 2
GATE 1
STORE OUT
MASTER CLOCK RESET
ZERO
J1


A15 LAMP ASSEMBLY
VDC
MVDC
VAC
Ω
KΩ
MΩ
DS1
DS2
DS3
DS4
DS5
DS6
R2 30
R5 30
R1 30
R6 30
R3 30
R4 30
KΩ CONTROL
Ω CONTROL
VDC CONTROL
MV CONTROL
VAC CONTROL
VAC RELAY
MV RELAY
Ω RELAY
+5V
MΩ RELAY
KΩ RELAY
VDC RELAY
S1
S2
S3
S4
S5
S6
MVDC
VAC
Ω
KΩ
MΩ
MV RELAY
ER RELAY
200V
POL
LOGIC COMMON
+5V
J12
CR15
15V
MV ZERO
REMOTE FUNCTION
MV CONTROL
VDC CONTROL
ER CONTROL
INPUT LOW
FILT
CR16







RANGE CODE				
RANGE	a	b	a	b
1	1	1	0	0
10	1	0	0	1
100	0	1	1	0
1000	0	0	1	1

NOTES.
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARDS UNLESS OTHERWISE SPECIFIED
2. ( ) DENOTES FRONT PANEL LOCATION.
3. ▼ DENOTES LOGIC COMMON.
4. HARD WIRED CONNECTOR CABLE MATES WITH J12 ON THIS ASSEMBLY AND CONNECTS TO J12 ON DISPLAY ASSEMBLY A12

FUNCTIONAL SCHEMATIC DIAGRAM

14

A13

INTERCONNECT ASSEMBLY

Drawing No. 8200A-1013 REV –

FLUKE JOHN FLUKE MFG. CO., INC.
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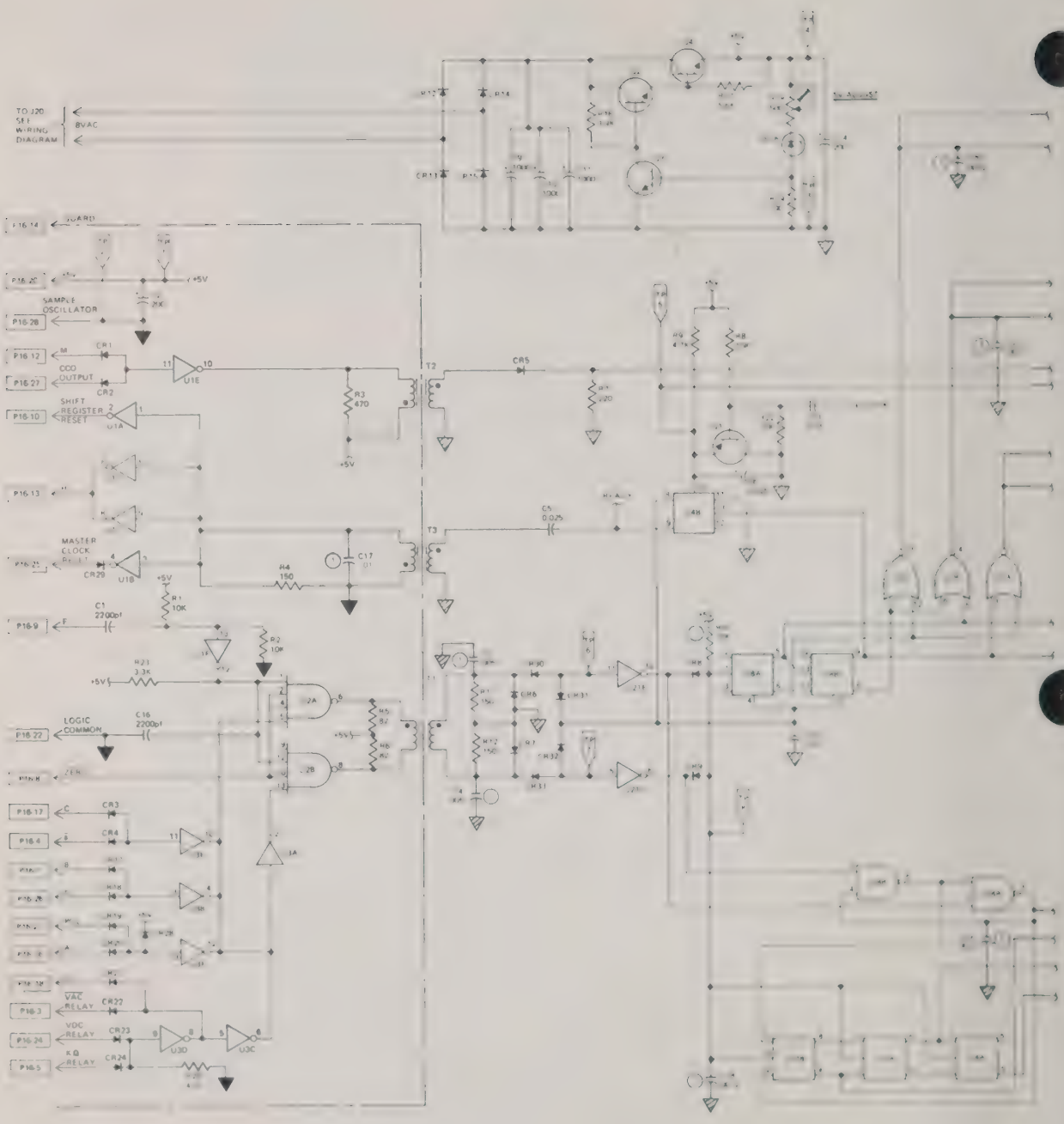
TO J20 SEE WIRING DIAGRAM
8VAC
P16-14
P16-26
+5V
SAMPLE OSCILLATOR
P16-28
P16-12
CR1
CCO OUTPUT
P16-27
CR2
SHIFT REGISTER RESET
P16-10
U1A
U1E
R3 470
T2
CR5
P16-13
MASTER CLOCK
P16-25
CR29
U1B
R4 150
C17 .01
T3
C5 0.025
C1 2200pf
P16-9
R1 10K
R2 10K
R21 3.3K
LOGIC COMMON
C16 2200pf
P16-22
P16-11
P16-17
CR3
P16-4
CR4
P16-18
P16-23
P16-19
P16-2
P16-20
P16-3
VAC RELAY
CR22
P16-24
VDC RELAY
CR23
U3D
U3C
P16-5
KΩ RELAY
CR24
R5 82
R6 82
2A
2B
3A
R1 15K
R12 15K
CR6
CR31
CR32
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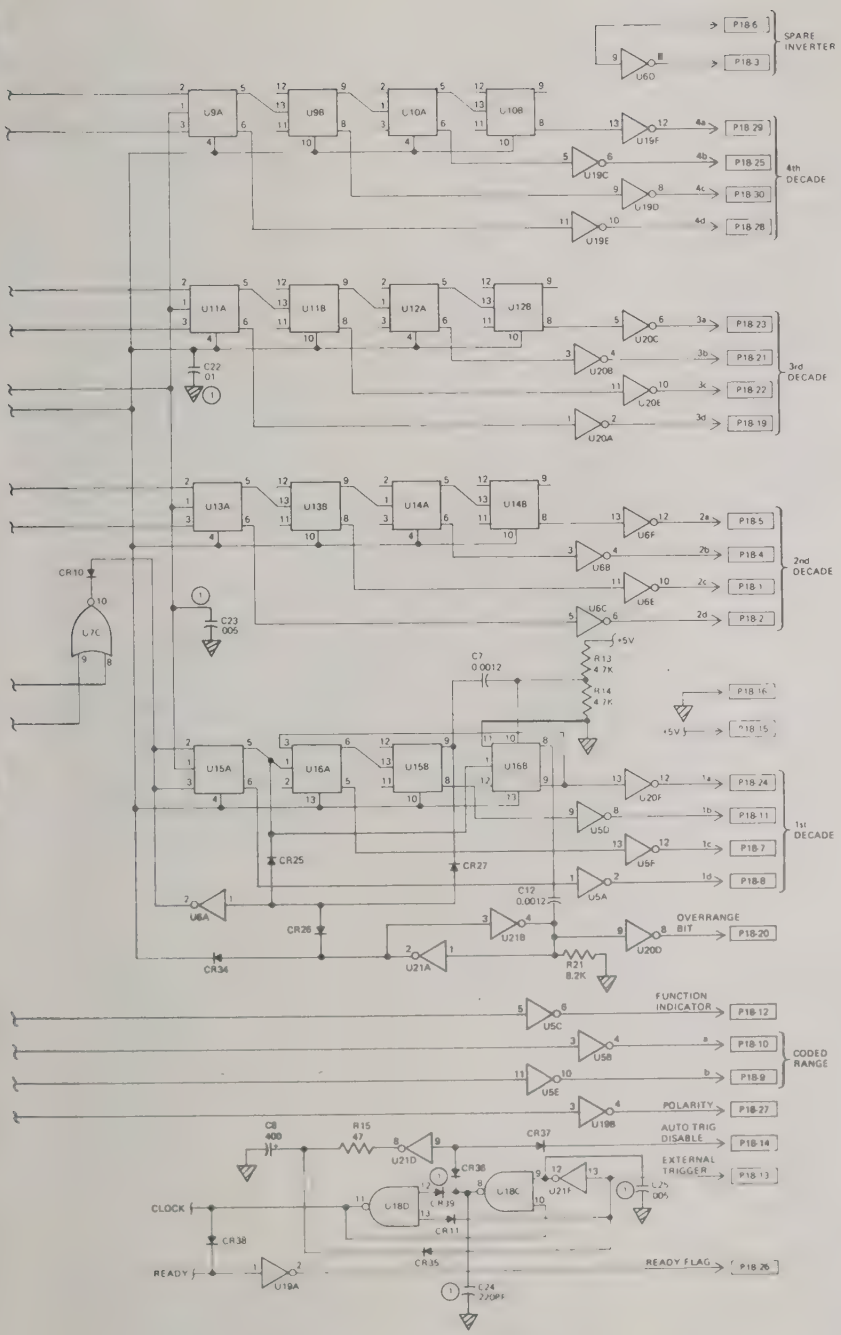
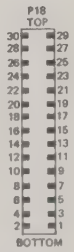


P18 PIN CONNECTIONS AS VIEWED FROM REAR OF INSTRUMENT



IC	PIN CONNECTIONS	
	+5V	COMMON
U1-U21	14	7

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. DENOTES LOGIC COMMON.
3. DENOTES EXTERNAL GROUND OR COMMON.
4. DENOTES INTERNAL ADJUSTMENT

CHANGES

(1) ADDED C3, C4, C17 THROUGH C25, R10, CR30 IN SER. NO. 173 AND ON.

FUNCTIONAL SCHEMATIC DIAGRAM

15

A16

PRINTER OUTPUT UNIT

Drawing No. 8200A-1016 Div —

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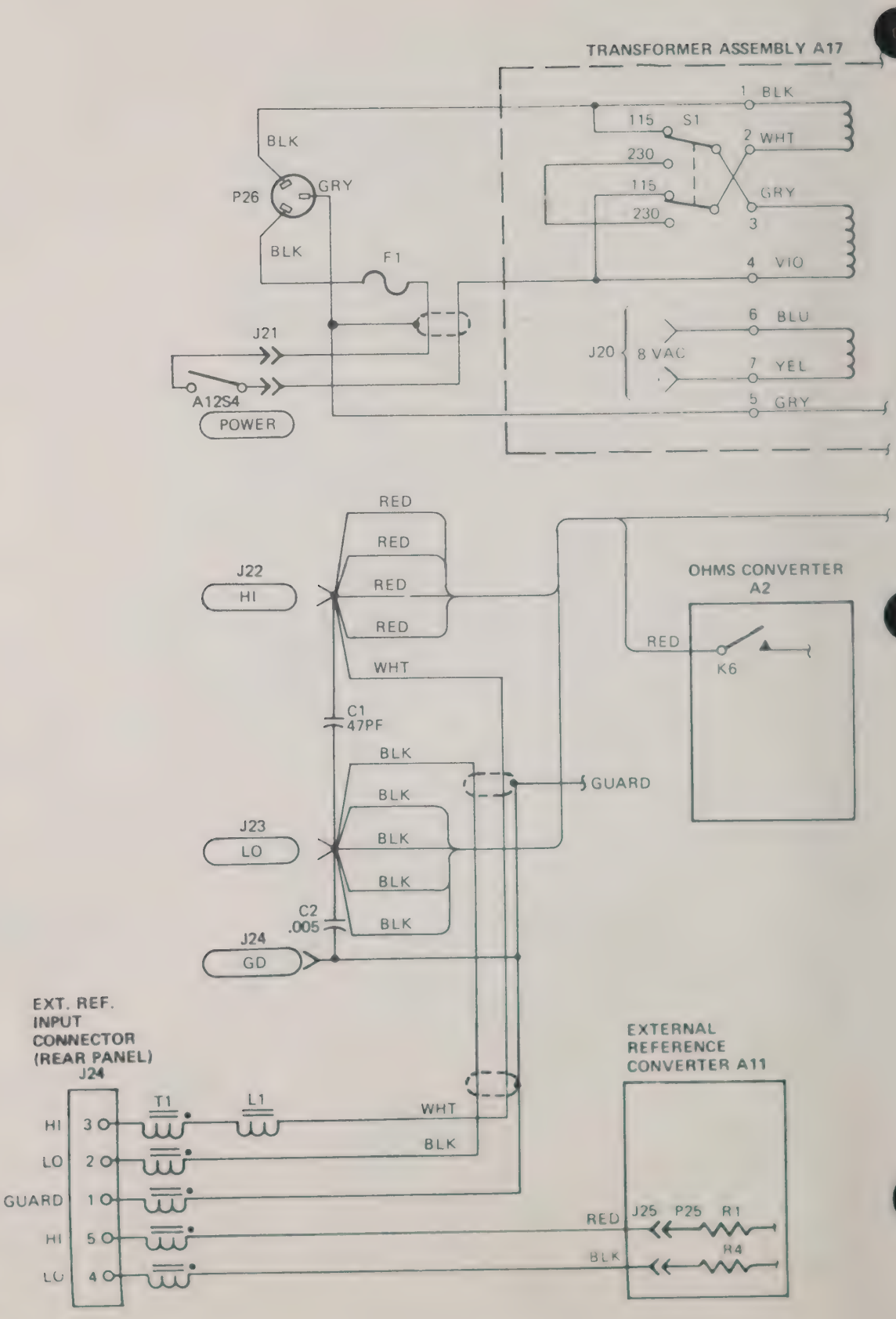
TRANSFORMER ASSEMBLY A17
1 BLK
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S1
2 WHT
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GRY
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4 VIO
BLK
P26
GRY
BLK
F1
J21
A12S4
POWER
J20
8 VAC
6 BLU
7 YEL
5 GRY
RED
RED
RED
RED
WHT
J22
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OHMS CONVERTER
A2
RED
K6
C1
47PF
BLK
BLK
GUARD
BLK
J23
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C2
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J24
GD
EXT. REF.
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(REAR PANEL)
J24
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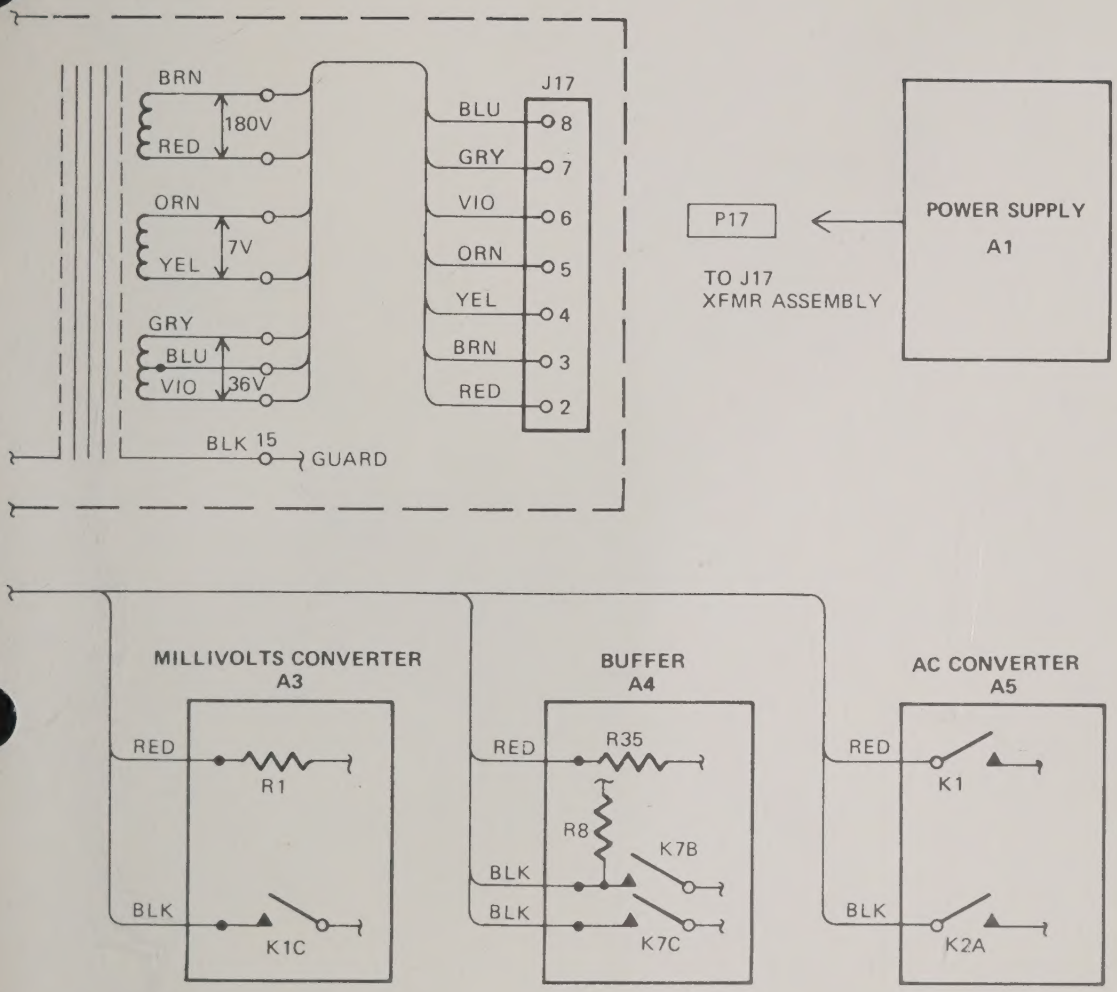
CONVERTER A11
T1
L1
WHT
BLK
HI 3
LO 2
GUARD 1
HI 5
LO 4
RED
J25
P25
R1
BLK
R4



NOTES:

1. ( ) DENOTES FRONT PANEL LOCATION.

CHANGES:

(1) ADDED T1, L1, C1, C2
IN SER. NO. 530 AND ON.

FUNCTIONAL SCHEMATIC DIAGRAM	
16 WIRING DIAGRAM AND INPUT POWER SCHEMATIC	
Drawing No. 8200A-1000	REV —
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

NOTES